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Development of a Bi-Directional Electronics Platform for Advanced Neural Applications

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Development of a Bi-Directional Electronics Platform
for Advanced Neural Applications

by

Luca Abbati

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
University of South Florida

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Stimulation, Low Noise Recording System

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When you see the final goal closer and closer the easiest thing to do is to keep on walking to get there, as fast as possible. But if you turn back for a second, you can see the enormous amount of people that helped you to get there, silently and patiently.

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ABSTRACT

This work presents a high-voltage, high-precision bi-directional multi-channel system capable of stimulating neural activity through bi-phasic pulses of amplitude up to ± 50 V while recording very low-voltage responses as low as tens of microvolts. Most of the systems reported from the scientific community possess at least one of the following common limitations: low stimulation voltages, low gain capabilities, or insufficient bandwidth to acquire a wide range of different neural activities.

While systems can be found that present remarkable capabilities in one or more specific areas, a versatile system that performs over all these aspects is missing. Moreover, as many novel materials, like silicon carbide, are emerging as biocompatible interfaces, and more specifically as neuronal interfaces, it becomes mandatory to have a system operating across a wide range of voltages and frequencies for both physiological and electrical compatibility testing. The system designed and proven during this doctoral research effort features a ± 50 V bi-phasic pulse generator, 62 to 100 dB of software selectable amplification, and a wide 18 Hz to 12 kHz bandwidth.

In addition to design and realization we report about biological testing consisting in the acquisition of neural signals from tissue cultures using an MEA where faithful signal recording was achieved with superior fidelity to a commercial system used to sample signals from the same culture. The only system parameter that was less robust than the commercial system was the noise level, which due to our higher bandwidth was somewhat expected. More importantly our custom electronics outperformed in terms of

lower delay and lower cost of realization. All of these results plus suggested future works are listed for the reader's convenience.

CHAPTER 1: INTRODUCTION

1.1 Basics of Brain Computer Interfacing

The acquisition and control of neuronal signals that propagate across the human body have been well investigated for several decades and is considered to be a very promising technology for both electronics and medicine. Common use of this technology involves neural circuits realized on silicon chips to build 'brain inspired' logic devices, the subsequent analysis of neural signals propagating across the body, the recording of complex neural activities, the restoration of neural pathways damaged after a trauma [1] or disease, and the study of the effects of drugs on the nervous system. An understanding of the mechanism behind the transmission of neural signals in the body requires a vast variety of concepts from many areas of research: from electrophysiology to neuroscience for interpretation of the signals, from electrical engineering to realize the electronic interfacing systems to signal processing techniques to acquire and recognize neural activity, from material science to medicine to understand and control how invasive implants can survive in the body's harsh environment and how the material's properties change over the course of the time.

Over the course of the years many methods have been presented to establish bidirectional communication with neural tissue from the human body and their feasibility have been proven *in-vitro*, *ex-vivo*, and *in-vivo*. A device capable of establishing a communication to and from the brain, a neural system or, more in general an electrically

active cell, is called the Brain Computer Interface (BCI) or, more in general, the Brain Machine Interface (BMI).

It is estimated that only in the United States almost 12,000 new cases of brain or spinal cord traumas are documented every year [2]. The patients that face these traumas are, in most of the cases, forced to be assisted in most of their daily activity and this significantly deteriorates the quality of life of both them and their families. Only a small percentage of these cases have been reported to recover to an almost normal life style after the injury occurs. Such numbers justify also a serious analysis of the economics behind the patient's health care. In many cases members of the family that are involved in assisting their loved ones must leave their jobs and their usual life style in order to help take care of the patient. These considerations clearly demonstrate how investments in such areas are strategic from a dual perspective – both economically as well as life style of those affected by neurological disease and trauma.

An important branch of biological research during the past few years has been aimed at reconnecting interrupted neural pathways by exploiting stem cells to regenerate nerves. The problem with this approach is that in nerve bundles there are hundreds, or even thousands, of parallel neural paths that connect different parts of the brain to the muscles or to the body receptors (i.e. tactile reaction). Such a huge number of parallel and independently operating pathways should be reconnected in such a way that the pathways before and after the injury are exactly restored. Brain auto-adaptive capability, known in the field of neuroscience as brain plasticity, is not able to fully map the badly connected paths and at the same time. At the present time, there exists no reliable biological control technique allowing stem cells to perfectly reconnect the corresponding pathways to each

other – an engineering solution to this vexing problem is clearly needed in order to provide near-term relief to thousands of patients suffering from neurological disease and trauma.

At a very high level, we can divide the different approaches for communication with electrically excitable cells in two categories: invasive and non-invasive devices. The most popular non-invasive interfacing technique is electroencephalography (EEG) [6],[7], where electrical activity of the brain is captured along the scalp (Figure 1.1). This approach requires external electrodes to be applied to the scalp and an external analog and digital processing unit to acquire, filter, amplify and interpret the electrical waveforms.

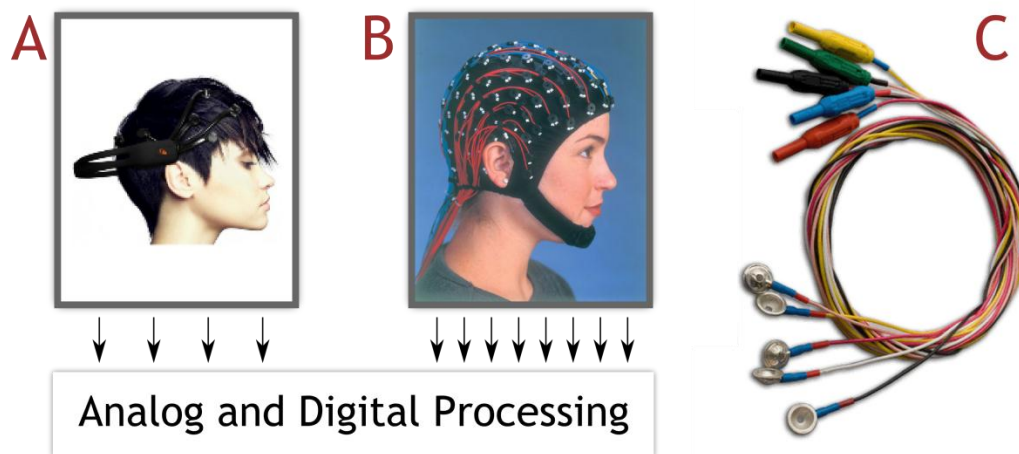


Figure 1.1 (A) Typical commercially available EEG system for consumer applications. (B) A typical EEG system suitable for research featuring a large number of points of acquisition and (C) typical electrodes used for acquiring brain activity. Image sources: www.jnetdirectbiosciences.com emotiv.com/, computace.blogspot.com, electrodes.sagura.com/

The main advantage deriving from the non-invasiveness of this method is the fact that it is fast to apply, does not present long-term side effects that could harm the person under test, is well established and is inexpensive. The main disadvantages are the fact that

it is unidirectional, i.e. it is only capable of recording spontaneously generated brain activity and cannot perform stimulation. In addition EEG offers a very low spatial resolution being largely limited by the maximum number of applicable electrodes. Another big disadvantage is that the subject using such a device must wear an uncomfortable scalp electrode array holder that can largely limit their movement. These kinds of systems have been demonstrated to be capable of accomplishing different tasks, such as, for example 1D and 2D pointer control on a PC display [8] or to navigate a wheelchair for paralyzed subjects [9].

On the other hand implantable invasive devices [10],[11],[12] allow for a higher spatial resolution and ideally, once installed, they are transparent to the user and work without restrictions. However such devices have to function with some stringent constraints in order to be implantable in the human body for a long period of time. First of all they have to be low power devices allowing for longer time periods between system re-charge during their normal operating periods. Second, they have to be biocompatible, i.e. they cannot be recognized as being foreign to the human body so that a localized immune system response is not induced by their presence.

Such systems have been successfully used in research experiments on animals to demonstrate their capability to control complex neural prostheses and systems. Figure 1.2 shows a typical 3D electrode array for implantation in the brain. Typically these systems consist of an array of electrodes that can be easily inserted within the cerebral tissue to establish bi-directional communication. Such systems have been proven to correctly acquire neural activity from the brain and have been used to control artificial prostheses after implantation in macaque monkeys (Figure 1.3).

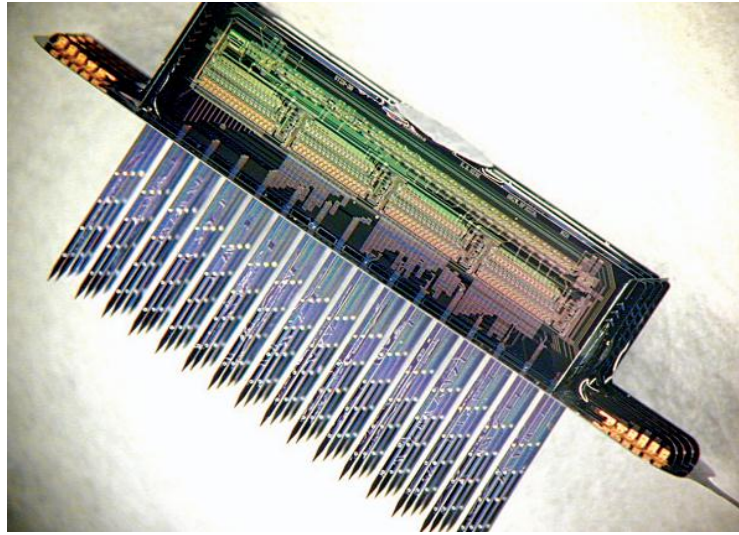


Figure 1.2 A 3D quad 64 electrode module for *in vivo* implantation from [10]. The system features both the electrodes and on board analog signal conditioning to increase signal-to-ratio by limiting the distance between the point of acquisition and amplification. © 2005 IEEE.

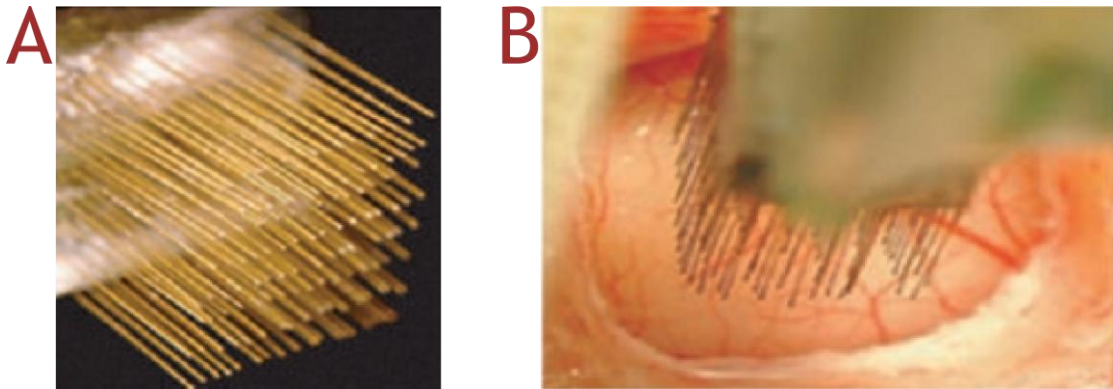


Figure 1.3 An implantable electrode array (source [12]) ready to be installed in a macaque monkey's brain. © 2003 PNAS.

1.2 Signal Propagation within the Body and Methods for Recording and Stimulation

While a deeper investigation of the electro-chemical phenomena behind the signal transfer within the body will be investigated more in depth in Chapter 2, it is worth to say now that such signals propagate in the body by means of electro-chemical action potentials (APs), i.e., a change in electrical potential between the inside and outside of an electrically-active cell that moves in a given direction along an electrically active cell [13]. We refer to intracellular recording when we have direct access to the internal volume of the cell and the measured voltage, V_m , is the potential difference between the inside and outside of the cell membrane $V_{in} - V_{out}$. We refer to extracellular recording when we measure a potential difference between an area in close proximity to the outside of the electrically active cell and a reference voltage, typically the potential of the electrolyte fluid in which the cell resides. Typically intracellular AP signals are in the order of tens of millivolts, while the extracellular recording range is from tens of microvolts to a few millivolts, with most of the information in the 100 Hz to 10 kHz frequency range.

The possibility of stimulating and recording APs simply by forcing intracellular (or extracellular) currents and the ability to read the AP through simple electrodes led, in the past few decades, to many research groups working in this field. Here is presented a review of the most interesting approaches and devices that exist in the literature to the present day to stimulate and to record action potentials. A more accurate examination of selected papers will be presented in Chapter 2 when the different methods to perform electrical characterization will be taken into account.

In the literature many different systems are reported that differ from each other from an architectural point of view, but from a biological point of view there are two underlying methods that really define the type of recording: Patch Clamping for intracellular recording and stimulation and microelectrode arrays (MEAs) for extracellular recording.

Patch Clamping [13],[14] consists of a pipette with highly resistant sides that is inserted, for example for voltage measurements, inside the cell volume. In a typical simple experiment the intracellular electrolytic medium can flow inside the pipette and a conductive wire is put through the pipette which serves as the electrical contact. The electrical potential of the inner cellular volume is transferred to a voltage or current amplifier and the output is connected to an oscilloscope. The oscilloscope reference voltage is kept at the electrolytic fluid voltage which is the potential of the extracellular space. When an electric action potential flows along the cell membrane and reaches the pipette, an electrical change in potential is detected and displayed on the oscilloscope.

This technique has been one of the first explored for the study of the cell membrane structure and electrical behavior. It allows very precise measurements of the electro-physiological phenomena that occur at the membrane electrolyte interface. The main disadvantage of this technique is the reduced number of patch clamps that can be used at once and the fact that it is strongly invasive for the cell, eventually forcing the cell to die.

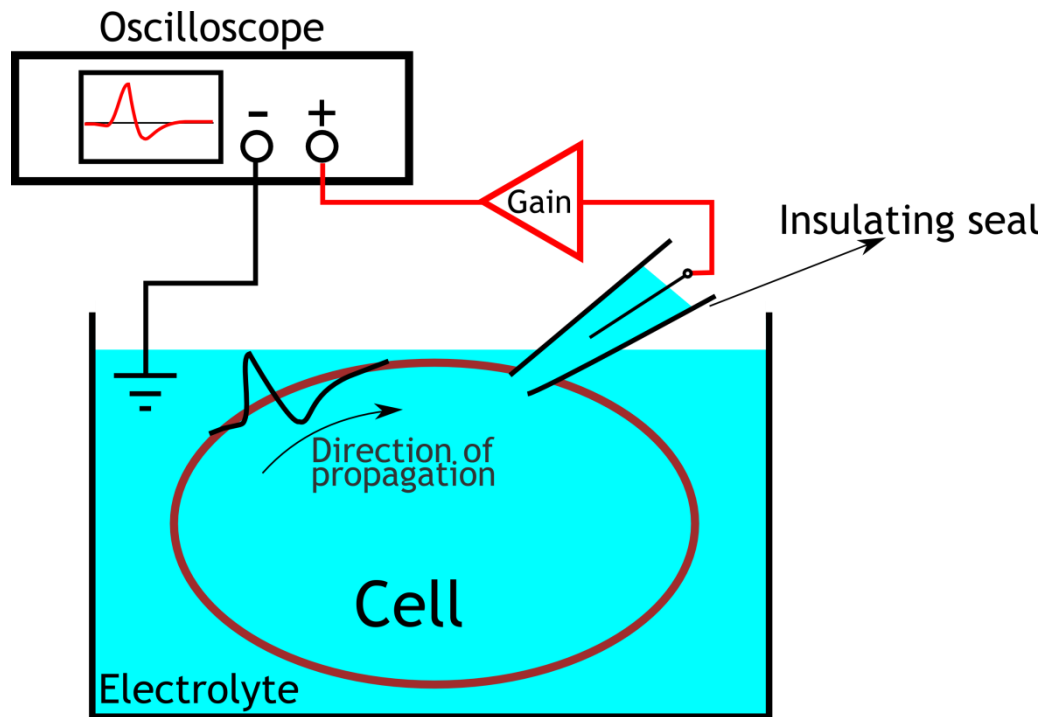


Figure 1.4 A typical simplified experimental setup for patch clamp (i.e., intracellular) measurements consists of an invasive voltage patch clamp with an high resistance seal ($R \sim G\Omega$), a current or voltage amplifier and a data acquisition instrument such as an oscilloscope.

An alternative approach developed lately to increase the number of recording sites is the Micro Electrode Array (MEA) approach which, as stated earlier, is an extracellular method.

In these devices a planar or three dimensional array of micron-scale electrodes are deposited on a bulk material, such as silicon. After the conductive material deposition that realizes the electrode, typically an insulating layer is deposited on the top to avoid short circuits of the signal traces due to the conductive electrolytic fluid. Neural or electrically active cells are then cultured on top of the MEA are plated on the top surface in close proximity to the electrodes. Indeed cells that are too distant from the electrode

will not contribute to signal recording, with a distance of a few micrometers, being sufficient to prevent recording from individual neurons at that distance.

Figure 1.5 shows a typical MEA application where the cells are cultured with different methods on an insulating material that covers the conductive traces which bring the signals away from the recording sites to the off-chip signal amplifiers.

In a typical system (Figure 1.6), the cell is placed in a conductive ionic fluid in close proximity to a planar electrode array. As the action potential flows along the membrane it causes a variation in the ionic concentration in the surrounding area. This variation is detected by the electrode and is amplified through a low noise amplifier (LNA) and filtered. A more in depth explanation of the physical and chemical phenomena that occurs at the membrane-electrode interface will be presented in Chapter 2.

The MEA approach is an *in vitro* technique and is non-invasive and allows for long term measurement of action potentials on a large scale.

Active Pixel Sensor Micro Electrode Arrays (APS-MEAs) are an interesting approach for high resolution recording of APs [15],[16],[17]. The APS-MEA consists of an array of micron scale gold electrodes that are integrated on a silicon chip (Figure 1.7).

Electrodes not covered by insulator

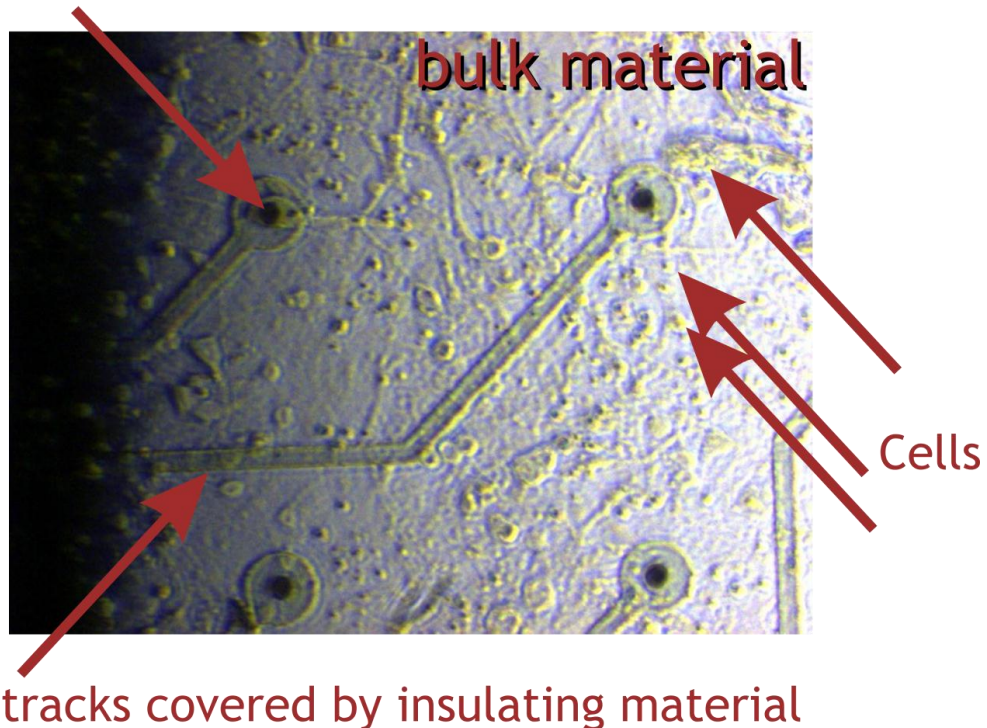


Figure 1.5 Optical microscope image of a typical micro electrode array (MEA) with the cells cultured on an insulating layer and the electrode traces underneath.

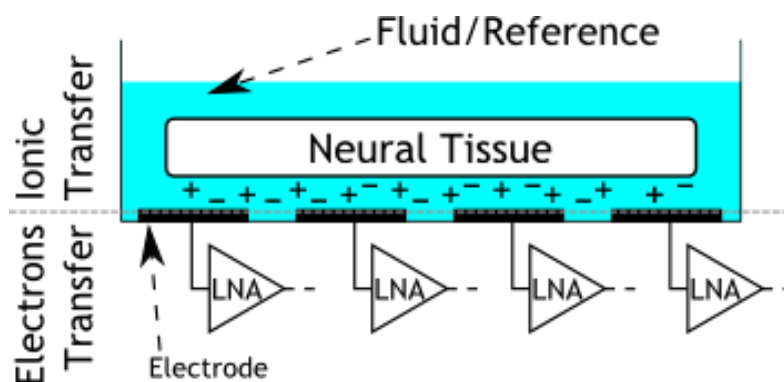


Figure 1.6 A simplified model of a typical MEA recording experiment. The electrical signals are passed from the membrane to an electrode by means of ionic current. The electrode is connected to a low noise amplifier, LNA, that can be at the recording site or in another area where the signal is to be filtered and amplified.

Electrodes consist of $20 \times 20 \mu\text{m}^2$ gold pads disposed with a pitch of $40 \mu\text{m}$. In every spot both the electrode and the preamplifier stage are integrated. This approach reduces the distance between the measuring electrode and the amplification stage, significantly improving the SNR of the signal. This device is realized with a standard $0.5 \mu\text{m}$ CMOS process on a silicon substrate. Depending on the number of micro electrodes the analog signal is sampled using a bank of ADCs and digitalized information is read with a FPGA based digital circuit. The usage of a FPGA allows for high speed data processing while reading the sampled signals out of the ADC bank.

The MEA approach presents a huge advantage in terms of spatial resolution and signal to noise ratio of the acquired signal. If the MEA is realized, like in this case on a silicon substrate, the first stages of filtering and amplification can be realized in close proximity to the electrode that is considered. The degree of filtering and amplification, and the bandwidth of the read-out circuit, is limited by the spatial constraints for a given resolution.

In [18] is presented an integrated circuit that features both recording and stimulation capability. This system features a bidirectional interface between the neurons and an electronic system. Both the analog front end for the recording and the stimulation are complex systems; therefore the filtering section is important in order to read out a signal that inherently has a low SNR ratio. The designer has to focus on the noise level at the amplification stage. Given the high gain needed, i.e. up to 100 dB, the risk of a high noise power at the output of the device exists. This risk is much more evident when the analog front end is moved from the same substrate of the electrode to an external PCB which presents, typically, long connection lines to the electrode pads.

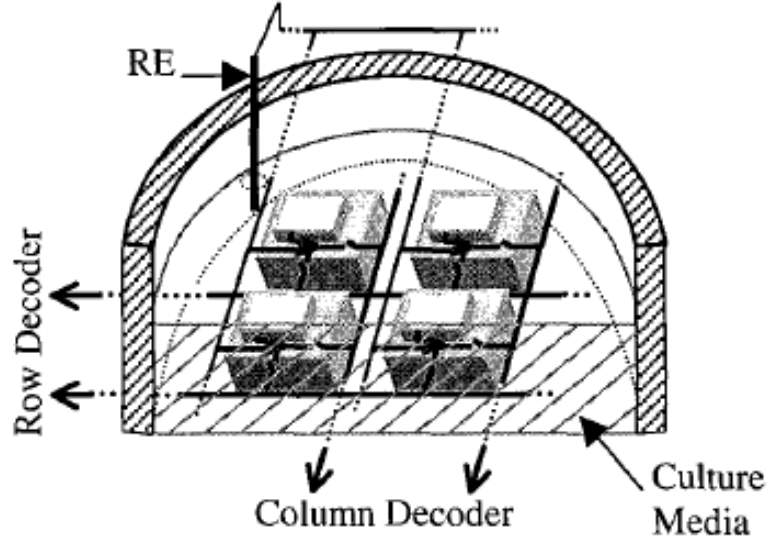


Figure 1.7 An overview of the Active Pixel Sensor Micro Electrode Array (APS-MEA) system, where the electrodes are in several rows and columns. The neural cells are placed in a solution which is used as the reference voltage of the system. © 2001 IEEE.

Stimulation of APs in neurons is not only realized by means of electric current or voltage pulses. In [19] optical pulses are reported to be capable of stimulating action potentials across the membrane. What the authors propose is a hybrid electrical-optic electrode, named an 'Optrode'. A tapered optical glass fiber termination is double coated with a thin gold (Au) layer and an electric insulator. A 440 nm light pulse is sent across the glass fiber which was reported to stimulate an action potential. APs can be recorded electronically using the same electrode and a set of other electrodes (Figure 1.8). The optrode is assembled on a commercially available device based on the Utah probe standard array architecture. The authors reported that they could stimulate the APs and simultaneously read signals from all the electrodes of the array at the same time.

While avoiding some phenomena typical of electrically generated APs (i.e., electrolysis at the electrode-solution interface when voltage pulses over 1 V are applied

[20][21]), this method has the disadvantage of requiring a biologically modified neuron. The activation of the AP arises because of a special light-sensitive protein channel called a Channelrhodopsin-2 (ChR2) [22]. This protein channel is native to seaweed and has to be biologically implanted in the neuronal tissue for optical stimulation to be possible.

Researchers have also investigated the possibility of transferring an AP signal between two neurons not directly in contact. In [1] authors were able to read a signal from neuron 'A' through capacitive coupling and, after a given amount of time, they were also able to stimulate the same AP to another neuron. This could be useful in a scenario where a neural path is broken because of an injury or an infection. With proper placing of such a system it would be possible to recover the full neural pathway in the damaged area and continue the propagation of the AP. A common characteristic of systems capable of reading APs is the very low noise profile, which should properly read voltages of tens or hundreds of microvolts.

Using stem cells researchers are able to restore neural path of a few centimeters in length. This is a very promising technique because, in principle, it is able to restore broken neural pathways without the implantation of a foreign alien device that can cause an immune system response. The main problem with this method is that an actual nerve bundle is typically made of hundreds or thousands of parallel neural fibers that bring information from the brain to a given muscle or receptor in the body. With restoring the neural path with stem cells there is no control over the mapping of the restored paths. Ideally, the i^{th} path before the damage should be reconnected to the same i^{th} path after the damaged area, channeling the correct flow of information from the brain to the final destination muscle or receptor. This is not possible because of the lack of control

methods during the growth of the stem cells. While it is true that the brain is capable of auto-calibration to restore some functionality (i.e., plasticity), it has been shown that this is not feasible when a large area of brain tissue is involved, due to the complexity of the neural network of interconnections. Electronic devices can play an important role in filling this gap.

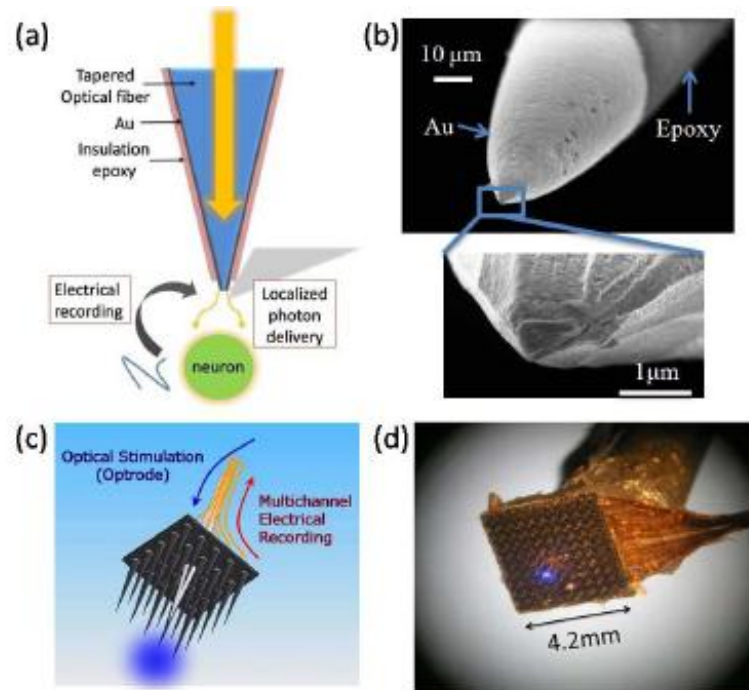


Figure 1.8 Optogenetics involves the stimulation of neural APs with light. (a) Concept schematic of single optrode. (b) SEM images of the optrode tip. The exposed metallic part of the tip is approximately 50μm, appearing brighter in the upper image. (c) Schematic of the hybrid device. The optrode is coupled to the MEA through a laser drilled hole. (d) An optical microscope image of the device, showing. © 2009 IEEE.

The task of acquiring and processing neural signals at low signal levels is complex and requires an extended signal processing capability. For this reason embedded systems have been proposed that are capable of stimulating and recording APs. An example is found in [23], where a 16-channel PCB-based acquisition system was proposed, entirely realized using off-the-shelf commercially available components. The

system consists of a pre-amplification and filtering section with a maximum gain of 94 dB and a bandwidth of between 445 Hz and 6.6 kHz. The architecture consists of 16 parallel analog stages that filter and amplify the signal before a 1 MSPS ADC. Information from the ADC is read using an external Complex Programmable Logic Device (CPLD) based system [24] which also controls the signals connection to the ADC stage. The main disadvantage of this architecture is that filtering of the signal at the analog front end limits the number of channels that can be read in the same system since, as the number of channels increases to hundreds, the space required for discrete components grows out of control. This makes this approach unsuitable for larger systems. Considering that often the read-out of useful information consists of hundreds of simultaneous channels, we can say that this approach is only valid for a limited scale research activity.

The solution adopted when the number of channels increases beyond, say, 16, is to transfer the analog front end with the filtering and amplification stage onto a chip, ideally within the same substrate as the micro electrodes interfacing with the cells. In [25] such a system was reported. In this architecture 64 channels are filtered and pre-amplified using the same number of integrated low noise amplifiers. Then all the channels are transferred to a dedicated PCB and time domain multiplexed (TDM) to an ADC. The values from the ADC are read using a fast FPGA, stored to a RAM and sent to a PC for further elaboration and visualization. This architecture allows for a larger number of channels while using off-the-shelf commercially available electronic devices.

1.3 Long-term Performance of Implanted Devices

While different systems found in the literature differ from each other from many points of view, all of them that are integrated circuits present a common characteristic:

the bulk material used to realize the electrodes or the underlying read-out circuitry is silicon (Si). In both the approach where only the electrodes are integrated, or the whole amplification stage is integrated, systems are realized typically with a standard CMOS process on a silicon substrate. Studies on silicon showed that long-term implantation of devices realized with this material results in failures of the device itself [26]. Figure 1.9 illustrates what happens at the electrode-brain interface after a certain time of implantation. The authors implanted different penetrating silicon electrode arrays, commonly known as the Utah intracortical array (or UIA) into a cat's brain and selectively analyzed both the recording signal quality and the physiological phenomena at the electrode brain interface. What they noticed is that after months both the electrical performance degraded and the electrodes were encapsulated in such a way that, in many cases, the device completely failed. This and other studies suggest that other materials have to be investigated in order to realize implantable and reliable devices able to withstand the human body's harsh environmental challenges and be perform for a time comparable to a human lifetime.

In [27] a comparative qualitative study of different materials in contact with brain cells was reported. Based on AFM investigation of the cells after a given amount of time in contact with the material, the authors assert that brain cells demonstrate a lower adhesion to silicon, which is qualitatively important additional evidence that silicon is not the preferred material for long term implantable biomedical devices. Silicon Carbide, on the other hand, represents a very promising alternative to silicon chips for the realization of long term implantable and biocompatible electrodes as shown in this study where a high degree of neural attachment was observed.

SiC is a well-known material used in many industries that that require operation in harsh environments [28]. It presents mechanical characteristics better than the silicon for micromachining purposes and it is possible to use fabrication processes compatible with standard IC devices, which makes the usage of this material a very promising choice. The confirmation of silicon carbide as a biocompatible material would open an incredibly interesting area of numerous biomedical device interests. This is because both the electrodes and the electronic circuitry could be realized on the same substrate with standard CMOS processes and, most importantly, the device could last for years, opening the way to a wide set of medical applications in the field of neural engineering.

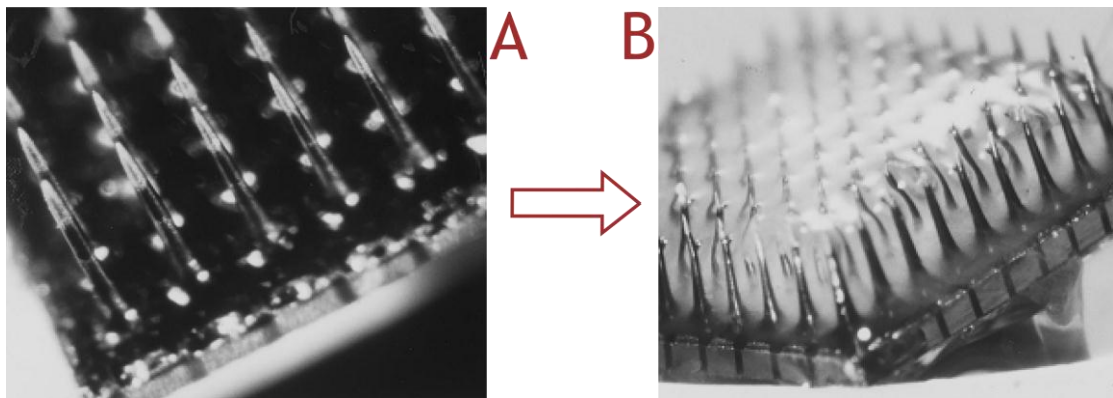


Figure 1.9 The UIA (a) before and (b) after implantation. Encapsulation of a silicon UIA after a few months in cat brain was observed. This phenomena causes a degradation or malfunctioning of the electrode electrical capability to record action potential, and eventually results in device failure after time. Image from [26].

1.4 Summary and Organization of Dissertation

In this chapter an introduction to the dissertation research that will be presented in the following chapter has been made. The motivation for the development of advance brain-machine-interface devices, including the ever important stimulation and recording electronics, has been made. Indeed, with thousands of new patients suffering from some form of neurological disease or trauma each year, and with the cost of medical care

skyrocketing, the need for low-cost, effective, long-term operable systems is clear. The main problem facing modern neuroengineers is the lack of a suitable biocompatible material that is more than just a plastic coating, such as polymers and other films, but is capable of performing sensing as well as supporting advanced electronics. This is critical since restoring neural pathways involves a high degree of neural signal processing, such as filtering and amplification, which can only be done with modern semiconductor platforms. In the USF SiC Group, Tampa, FL, a long history of exploring SiC for biomedical applications has been assembled [58] and, more recently, focused research on developing biomedical devices for neurological applications has been on-going [60]. Based on the early work done by Coletti [59], that demonstrated the biocompatibility of SiC to skin and connective tissue in-vitro, and follow-on work by Schettini [61] that demonstrated that 3C-SiC was hemocompatible, Frewin set out to prove that 3C-SiC was suitable for the neural environment [60]. Perhaps the most interesting outcome of his work was the demonstration that 3C-SiC was far superior to diamond for neural compatibility in-vitro, and when primary neurons were used this material performed equally to polyimide, the gold standard of neurocompatible materials at that time. The USF SiC Group had fabricated 3C-SiC MEA's but was in need of a low-cost, highly effective electronics platform to perform in-vitro experiments (in the first stage) and, eventually, to use in in-vivo studies (in the next stage of research). With this need this dissertation was born with the goal of assembling a highly effective, bi-directional electronics platform for these applications.

The dissertation is organized as follows. After the introductory chapter which was summarized above, Chapter 2 discusses the theory behind the electrical signal

transmission across the body and the mechanisms that determine the generation and propagation of action potentials. Moreover in Chapter 2 I will present a review of a few different existent systems from the literature that have been successfully tested for neural recording and I will individually highlight the most significant features that each of them shows.

Chapter 3 will report on the system specification of the custom electronics we designed, with an complete overview of the many different parts that together compose the system. The chapter is divided in basically three parts, an initial part about the motivations and the specifications we were imposed, a second part with the design and simulation of the electronics boards and a third part showing the FPGA firmware for the control unit that coordinate and synchronize the whole system during both stimulation and recordings.

Chapter 4 will summarize the test that we made to validate the architecture. Firstly, a complete electrical test and characterization have been performed with an accurate measurement important parameters like the gain, the bandwidth and the input referred noise: such measurements, will be compared with the values expected from the simulations performed. Secondly, the system has been tested *in-vitro* with both dissociated neural cells and C57BL/6J hippocampal brain slices.

Chapter 5 will summarize all the work done and propose some possible path to improve and complete the system that presents many possible evolutions in both the analogical electrical part and the software used to manage it.

CHAPTER 2: PHYSIOLOGY OF EXCITABLE CELLS AND INTERFACING METHODS

2.1 The Cell Membrane

The membrane of a cell is a layer that separates the cellular internal and external volumes, which are called, respectively, the intracellular and extracellular areas [13].

Figure 2.1 shows a schematic overview of a limited portion of the cell membrane.

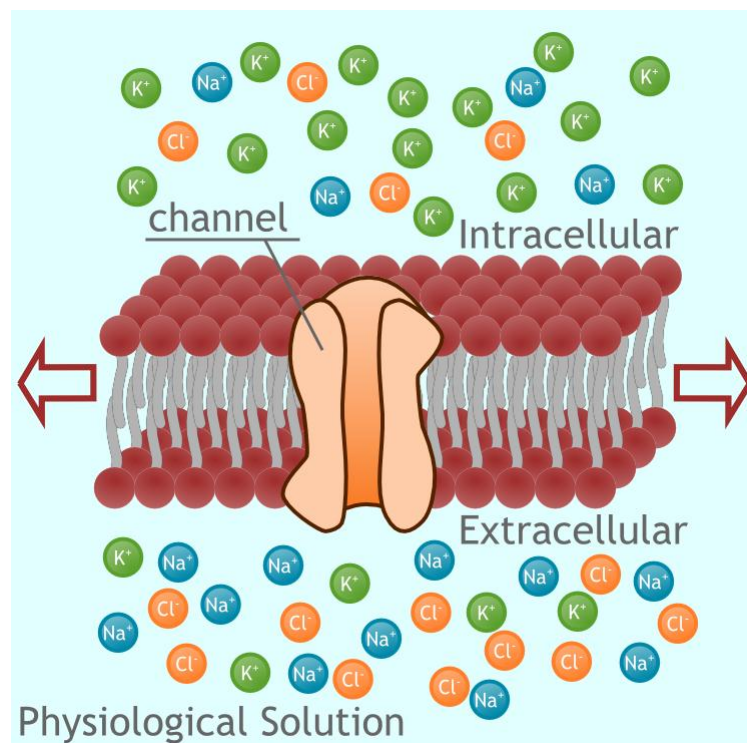


Figure 2.1 A schematic representation of the cell membrane that divides the cell's intracellular and extracellular volumes (not to scale). Typical membrane dimensionless than 100 Å with a typical thickness of the internal lipidic layer of 30 Å, while an ion diameter can be as low as 1 Å. The ions in the image are sodium (Na⁺), potassium (K⁺) and chloride (Cl⁻). There are other ion species but these are the ones that play the most important role, with Na⁺ and K⁺ dominating over the others.

The cell membrane is mainly comprised of a double lipid layer, that blocks the transfer of ions across the membrane, and complex protein assemblies that comprise the so called membrane *channels* and *pumps*, whose main function is to regulate the transfer of ions across the membrane. Ions are the unique mechanism of conduction across the membrane, the most important ion species are sodium (Na⁺), potassium (K⁺) and chloride (Cl⁻) with the first two being the most important for the physical propagation of action potentials (Aps). Ions are present in the physiological fluid representing the cell's environment in different concentrations in the intracellular and extracellular volumes. The lipid layer prevents the passage of ions between these two areas, acting as an insulating layer from the electrical point of view. Both *pumps* and *channels* are typically selective, i.e. they permit the passage only of specific ion species and contribute to the overall equilibrium between the intracellular and extracellular spaces, with the difference being that the *pumps* move ions against their natural flow, while the *channels* permit the passage of species according to their natural flow, as explained in the next sections.

The intracellular and the extracellular spaces permit the movement of charged ions, while the lipid layer prevents the ions from going through. This assembly can be electrically modeled as an electrical insulator, the lipid layer that divides the two conductive areas, the intracellular and extracellular spaces. From an electrical point of view this is perfectly equivalent to a capacitor and is named the *transmembrane capacitance*, C_m , per unit of area

$$C_m = \frac{ke_0}{d} \quad (2.1)$$

where k is the dielectric constant, ϵ_0 is the permittivity and d is the membrane's insulating layer thickness. Typical values for the parameters above are $k=3$ and $d=30 \text{ \AA}=3 \text{ nm}$ that gives a typical transmembrane capacitance value of 0.9 \mu F/cm^2 .

2.2 Ionic Currents in the Solution and Through the Membrane

Ions move in a solution that permits their mobility because of two causes: differences in concentration between two points in space or an electric field. Differences in spatial concentration of a given ion cause all of the molecules of that ion species to move in order to have, as a final result, a flat constant concentration all across the available space. This process, known as *diffusion*, arises mainly because of the thermal energy store in such ions. The process of diffusion, and in particular the flux of a given ion species through a section of unity area, can be quantitatively described by the Fick's law:

$$\bar{j}_d = -D\nabla C \quad (2.2)$$

where D is a constant dependent on the solution and the particular ion that is typically determined from experiment and C is the localized concentration of a particular ion. J_d is the current density in A/cm^2 .

Ions are charged particles, which means that they are sensitive to electric fields and that they move consequently. Different ions present a different atomic number and, therefore, a different mass and dimension. For this reason different ion species shows a different *mobility* when they encounter an electric field in solution. *Mobility* is defined as the maximum velocity that a given ion can reach in a specific solution when a unity electric field is constantly applied to it. The ionic flux of the i^{th} ion in a given solution is given by the law

$$\bar{J}_e = -u_i \frac{Z_i}{|Z_i|} C_i \nabla \Phi \quad (2.3)$$

where u_i is the i^{th} ion mobility, Z_i is its valence, C_i is its localized concentration and $\nabla \Phi$ is the applied electric field in the particular point of interest. Even in this case the flux represents the number of ions flowing through a unit area cross section.

The diffusion constant, D , and the mobility, u , are related by Einstein's law

$$D_i = \frac{u_i RT}{|Z_i| F} \quad (2.4)$$

for the i^{th} ion species where R is the gas constant, F is Faraday's constant and T is the absolute temperature.

The resulting flux of ions that arises from the superposition of the two phenomena for the i^{th} ion species is

$$\bar{J}_i = \bar{J}_d + \bar{J}_e = - \left(u_i \frac{Z_i}{|Z_i|} C_i \nabla \Phi + D \nabla C_i \right) \quad (2.5)$$

which, combined with (2.4), gives the *Nernst-Planck* equation

$$\bar{J}_i = -D \left(\frac{Z_i C_i F}{RT} \nabla \Phi + \nabla C_i \right). \quad (2.6)$$

This value can be multiplied by the number of charges in each mole $Z_i F$ to obtain a current density

$$\bar{J}_i = Z_i F \bar{J}_i \quad (2.7)$$

which represents the current per unit of area of the cross section that the ion flux goes through.

2.3 The Parallel Conductance Model of the Membrane

The potential difference, V_m , between the internal and the external surfaces of the membrane is called the *transmembrane potential* and is defined as

$$V_m = \Phi_i - \Phi_e. \quad (2.8)$$

The value of this potential difference at resting condition varies between different types of excitable cells. As a reference we can assume that a typical value for V_m is -60 mV and that it does not exceed ± 100 mV. Even if this is a relatively low voltage, the value of the electric field across the membrane is very high due to the very thin layer over which this potential difference is measured, i.e. the membrane thickness which is well below 100 Å.

2.3.1 Membrane Permeability and Nernst Equilibrium

Figure 2.2 shows a typical concentration cell useful to study the dynamics of ions moving across two regions of a volume with different concentrations. Ions are assumed to be equally concentrated in their region, the membrane is permeable only to one ion species P^+ while the other species Q^- cannot pass through.

Assuming that at the time t_0 the P and Q ion concentration in the same compartment are the same, the transmembrane voltage V_m is 0 V because on each side of the membrane there is the same amount of positive and negative charges. As time passes, P^+ ions start to move from the intracellular to the extracellular compartment because of the concentration difference. V_m is then given by

$$V_m = \Phi_i - \Phi_e = \Delta P^+ / C_m \quad (2.9)$$

where C_m is the membrane capacitance and ΔP^+ is the number of P^+ ions that moved from the intracellular to the extracellular space.

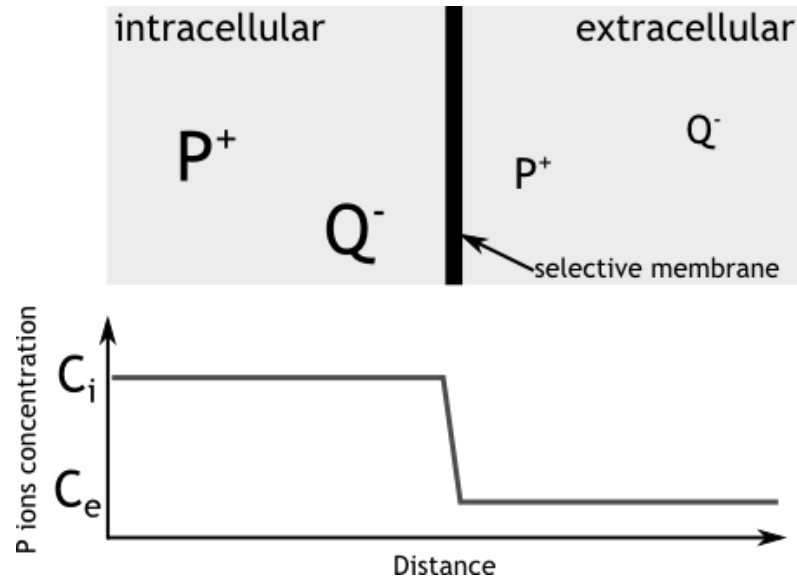


Figure 2.2 A permeable membrane separates two volumes called intracellular and extracellular. In both volumes two hypothetical ion species are present, P^+ and Q^- , with P^+ and Q^- ion concentration in the intracellular area being larger than the one in the extracellular area. The selective membrane is permeable only to P^+ ions.

Assuming the membrane to be a perfect insulator, we have that the electric field across the membrane is

$$E = \frac{V_m}{d} = \frac{\Delta P^+}{C_m d} \quad (2.10)$$

where d is the membrane thickness. The relation above affirms that as more and more P^+ ions leave the intracellular volume, an electric field is formed whose direction is from the extracellular toward the intracellular space. This field clearly works against the movement of positive charges due to the concentration difference until the two different phenomena reach an equilibrium characterized from the total current density \bar{J}_p for the ion P^+ to be null. From (2.7) we have that for $\bar{J}_p = 0$

$$\nabla C_p = -\frac{Z_p C_p F}{RT} \nabla \Phi. \quad (2.11)$$

Considering only the dimension perpendicular to the membrane surface and integrating the relation above and transforming the natural logarithm to the base 10 logarithm we obtain the relation between the transmembrane potential V_m and the concentration at the equilibrium, also known as the *Nernst Potential*, for the P^+ ion:

$$V_m^{eq} = \frac{58}{Z_p} \log_{10} \left(\frac{[C_p]_{external}}{[C_p]_{internal}} \right) \quad (2.12)$$

with V_m^{eq} being typically around 100 mV.

For the main ion species involved in the transmission of APs we can say that at equilibrium they have a specific *Nernst Potential* that combines to give the overall resulting V_m . We can call these values E_{Na} , E_K and E_{Cl} that are based on typical measurements as shown in Table 2.1, which are positive, negative and negative, respectively (the chloride has an external concentration that is larger than the intracellular, but its valence is -1).

Assuming that channels in the membrane are selective, i.e. are permeable under certain conditions to only one species of ion, we can say that, based on the number of channels opened at a certain point in time for a given ion, the i^{th} ion experiences a given *transmembrane conductivity* which is a quantitative indication of how many ions can flow through the membrane at a given time t . The superposition of this consideration for the three species gives the *equivalent parallel conductance model* for the cell membrane (Figure 2.3).

Table 2.1 Typical experimental intracellular and extracellular concentrations of the main ion species from a squid axon nerve [13].

	<i>Intracellular mM</i>	<i>Extracellular mM</i>
K^+	397	20
Na^+	50	437
Cl^-	40	556

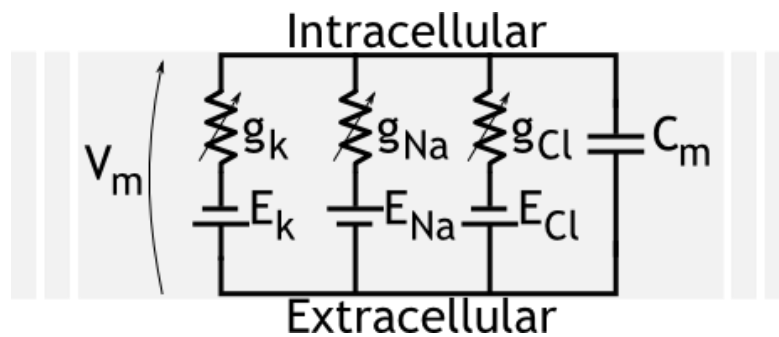


Figure 2.3 The parallel conductance equivalent model of the cell membrane. C_m is the membrane capacitance per cm^2 , g_k , g_{Na} and g_{Cl} the membrane conductance for the respective ion and E_k , E_{Na} and E_{Cl} the Nernst Potential for the single species. E_k , E_{Na} and E_{Cl} in this figure have to be intended as positive numbers and the polarity of the voltage source gives the direction. The actual V_m is the result of the superposition of the three branches.

The current on each branch is given by

$$I_i = g_i(V_m - E_i) \quad (2.13)$$

where E_i is considered with the proper sign. At the same time the current I_c through the capacitance is

$$I_c = C_m \frac{dV_m}{dt} \quad (2.14)$$

At resting condition the voltage V_m is constant, I_c is null and the total net current must be zero. This condition gives:

$$I_m = 0 = I_{Na} + I_K + I_{Cl} \quad (2.15)$$

which when combined with (2.13) for each ion species gives the *parallel conductance equation for the resting transmembrane potential*

$$V_m^{rest} = \frac{g_k E_k + g_{Cl} E_{Cl} + g_{Na} E_{Na}}{g_k + g_{Cl} + g_{Na}}. \quad (2.16)$$

2.4 Membrane Structure and Channels Conductance

The cell membrane's double layer of lipids presents a very high resistance to the passage of ions with an electrical resistivity on the order of $10^9 \Omega\text{-cm}^2$. Due to this layer the ions would be confined to their respective volume. Spread along the membrane are complex proteins that have a structure that can selectively let ions of a specific species pass through. These proteins are called *ion channels*. When channels are present on the membrane and they are opened, the localized membrane resistance varies considerably down to $1 \text{ k}\Omega\text{cm}^2$ from $10^9 \Omega\text{-cm}^2$. The opening and closing of such channels can depend on different parameters, with voltage across the membrane and ion concentration being the main ones. Figure 2.4 shows a schematic view of the lipid bilayer and the protein that realizes the ion channel. A typical channel consists of a *gate* to enable or disable the passage of ions, a sensor to sense different parameters such as the voltage and ion concentration in order to set the state of the channel between open and close, a filter to block ions different from the species of interest, and a aqueous channel that is the actual conductive path for the ions through the membrane.

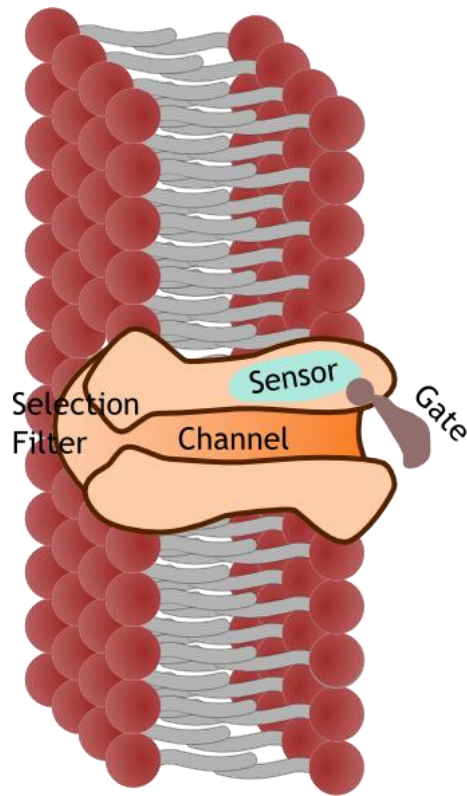


Figure 2.4 A schematic representation (not to scale) of a typical ion channel. The proteins locally replace the lipid bilayer and selectively filter ions based on voltage or concentration differences, among others. A typical channel can be as low as 2 nm in diameter.

2.4.1 Currents Through a Single Channel

Based on the parallel conductance model, we can say that for the single channel (e.g., we consider a potassium channel) the current can be written as

$$i_k = \gamma_k(V_m - E_k) \quad (2.17)$$

where γ_k is the conductance of the single potassium channel. A typical value measured for γ_k when the channel is open is 20 pS, i.e. 50 G Ω . When many of these channels are open at the same time, the membrane resistance of 1 k Ω cm² can be measured. Assuming

this value for the potassium conductance of the single channel and a $(V_m - E_k)$ of 50 mV we can see that the corresponding current is $i_k = 2$ pA.

Fortunately this current value is large enough to be measured with a sufficiently good signal to noise ratio (SNR). In order to prove this assertion we calculate the *Johnson noise* for the current in a 50 G Ω resistor which is

$$\sigma_n = \sqrt{4kT\Delta f/R} \quad (2.18)$$

which, on a 1 kHz band, gives a noise of 0.02 pA_{RMS} which is extremely low compared to the signal of 2 pA.

2.4.2 Voltage and Patch Clamps

Measuring the current for a single membrane channel is extremely challenging for two reasons: the dimension of single channels are on the order of nanometers, and the channel resistance, even when the channel is open, is extremely high.

Figure 2.5 shows how a poor membrane-pipette interface can compromise electrical measurements. The channel resistance that we intend to measure is in the order of gigaohms while a poor contact could cause leakage resistances, R_{seal} , as low as tens of megaohms. It is clear that in this case the SNR of the measurement would be completely compromised. Fortunately nowadays patch clamping techniques exist with diameters lower than 1 μm and R_{seal} values higher than 100 G Ω that enable such experimental measurements.

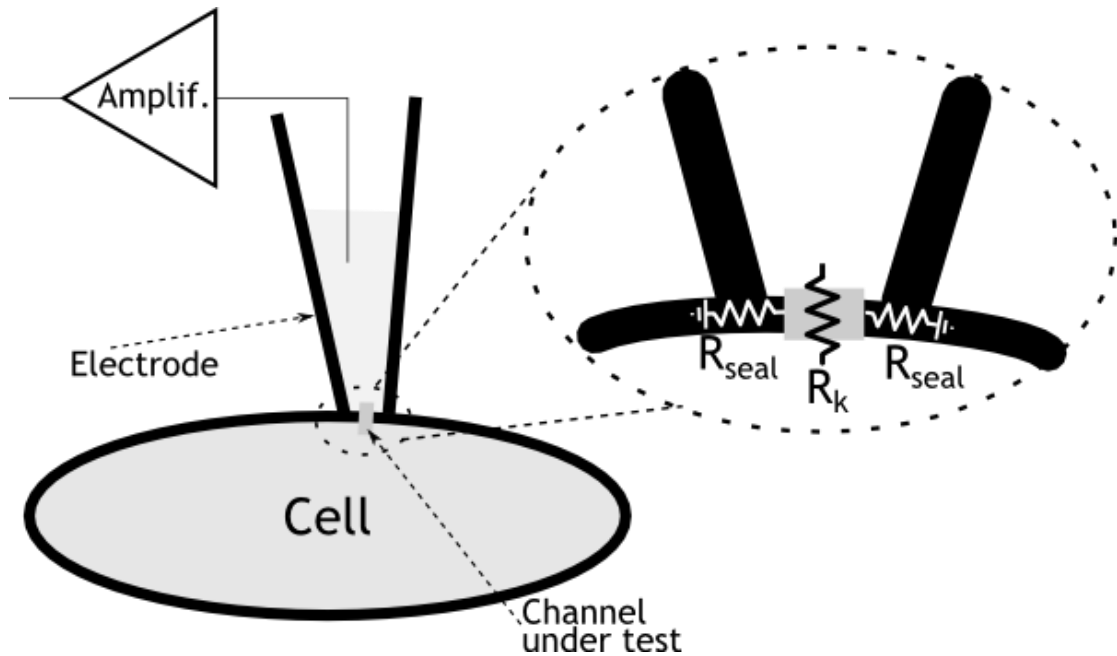


Figure 2.5 An illustration of the electrode-membrane interface. The electrode consists of an insulating pipette in touch with the cell membrane. The insulating seal is necessary to protect the internal electrode from the conductive surrounding fluid. R_k is the resistance of the potassium channel, R_{seal} are the leakage resistance of the electrode.

Figure 2.6 shows an experimental recording from giant squid axons measured with patch clamp techniques. When a voltage step of 150 mV is applied, a current of around 2 pA is measured. The number of tracks from different measures in different locations shows that the channel acts like a switch, being either open or closed. The figure also shows that the ensemble mean of different measurements results in the expected behavior. This result suggests that a simplified electrical model of an open channel, for example the potassium channel, could be a fixed resistance r_k in series with the Nernst potential E_k in series with a switch as Figure 2.7 shows.

The opening and closing of the channel is a stochastic process that is the key to understand a mathematical model explained in the following sections. An ensemble of opening and closing channels regulate the propagation of the APs across the cell

membrane. The transmembrane potential V_m causes the ion channels to open and close, at the same time open and closed channels can, or cannot, block ions from moving from the intracellular to the extracellular volumes and vice versa, thus modifying V_m . This closed loop is at the base of the transmission of the APs in the cell.

Once opened, a channel demonstrates that it behaves as an ohmic channel with current through it proportional to the voltage V_m .

The channel conductance can slightly vary for different species and cells typically between a few to hundreds of picosiemens, while the distribution is from a few to thousands of channels per square centimeter of membrane area.

2.5 The Hodgkin-Huxley Membrane Model

In the early 1950s Hodgkin and Huxley (HH) developed a mathematical model, since named after them, to explain and predict the behavior of channels during APs [29]. For these studies they were awarded the Nobel Prize in 1963. This model is a statistical model and, in order to prove it, they developed a special voltage/space clamp that let them measure the propagation of an action potential in a very accurate way. This section presents a quick and non-exhaustive overview of the HH model and its consequences.

Assuming a membrane area containing N channels of which an average number $\langle N_o \rangle$ are open and an average number $\langle N_c \rangle$ are closed, we can define:

$$p = \frac{\langle N_o \rangle}{N} \quad (2.19)$$

$$q = \frac{\langle N_c \rangle}{N} \quad (2.20)$$

$$p + q = 1 \quad (2.21)$$

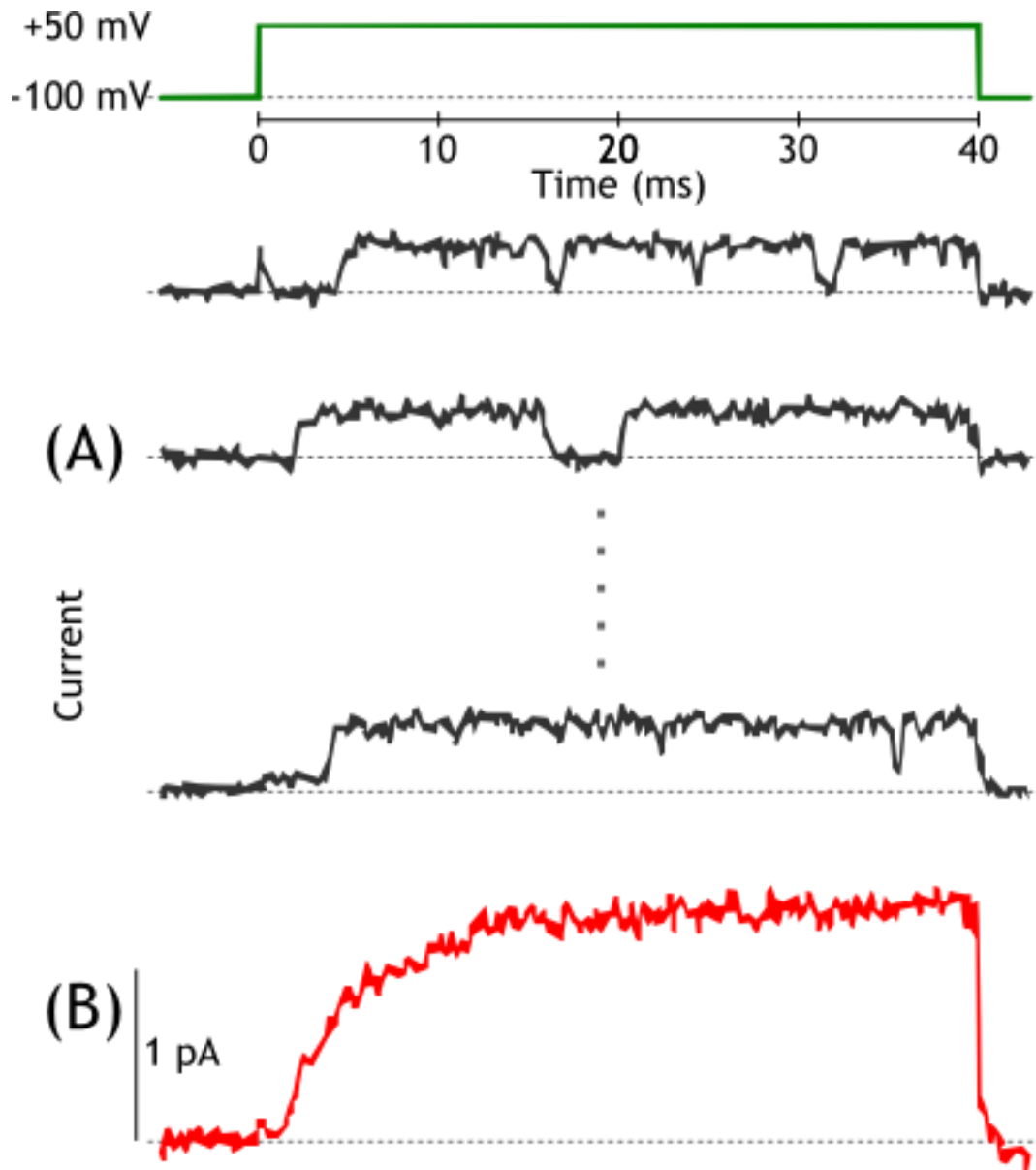


Figure 2.6 An example of patch-clamp recording of unitary K currents in a squid giant axon during a voltage step from -100 to 50 mV. (A) A number of consecutive trials showing channels of 20 pS conductance filtered at 2 kHz bandwidth. (B) Ensemble mean of 40 repeats; these reveal the expected macroscopic behavior. $T=20^\circ\text{C}$ [13].

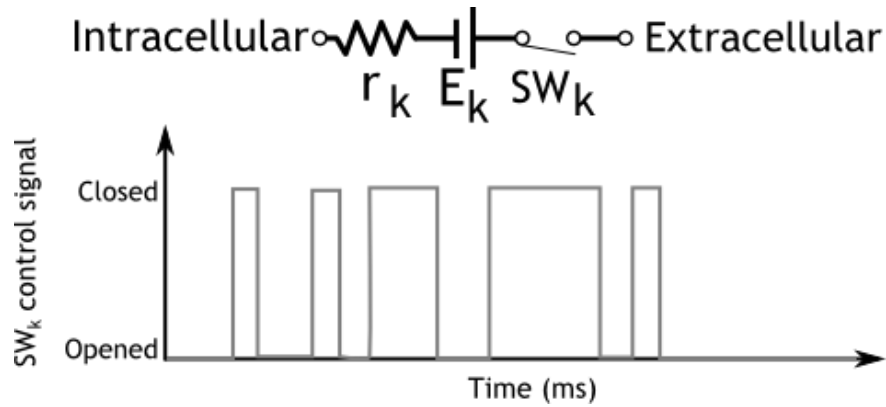


Figure 2.7 A simplified model of a signal potassium channel with a constant resistance r_k of $50 \text{ G}\Omega$ (or g_k of 20 pS), the Nernst potential E_k and a switch that is closed (or opened) in response to the changes in concentrations and membrane voltage V_m .

where p and q are the probabilities that a single channel is closed or open, respectively.

For the single channel, for example a potassium channel, we know from the parallel conductance model that

$$i_k = \gamma_k (V_m - E_k). \quad (2.22)$$

Then, at a macroscopic level, the current through an area of membrane is considered to be

$$I_k = N p_k \gamma_k (V_m - E_k). \quad (2.23)$$

The model of HH shows that the total membrane current can be derived as the sum of currents from single ions. They made the assumption that a channel is formed by subunits called *particles* of different types. These units are more mathematical than physical entities. They assumed that a potassium channel is considered open only 4 particles of type n from this channel that have moved from closed to open. In the case of sodium they assumed that a channel is considered open only if 3 particles of type m and 1

particle of type h have moved from closed to open. We can define the probabilities that a single channel is open as

$$p_k = n^4 \quad (2.24)$$

$$p_{Na} = m^3 h \quad (2.25)$$

where n , m and h are the probability that the single channel is open.

Focusing on potassium channels, we can say for the single particles the transitions from closed to open are regulated by a dynamic first-order process with a rate constant α for going from closed to open and a rate constant β for going from open to closed

$$\frac{dn}{dt} = \alpha_n(1 - n) - \beta_n n \quad (2.26)$$

where $(1-n)$ are the number of closed particles. This differential function can be solved and shows the evolution in time of the number of open particles. With this in mind we can consider that we have the maximum conductance at a macroscopic level when all the N channels that we are considering are open, thus for the potassium channels

$$\overline{g}_k = N\gamma_k \quad (2.27)$$

and recalling (2.24)

$$g_k = \overline{g}_k n^4 = N\gamma_k n^4 \quad (2.28)$$

where

$$I_k = g_k(V_m - E_k) \cdot \quad (2.29)$$

For the sodium channels a similar process yields

$$g_{Na} = \overline{g}_{Na} m^3 h = N\gamma_{Na} m^3 h \quad (2.30)$$

and

$$I_{Na} = g_{Na}(V_m - E_{Na}). \quad (2.31)$$

Using the HH model it is possible to predict the evolution of the channels opening over time with a very good precision. This study opened the way for a vast range of different research and to a more comprehensive comprehension of the mechanism behind the AP generation and propagation.

2.6 Action Potentials

With the membrane structure and the channel characteristics in mind, we can define an action potential as a rapid membrane depolarization due to a fast inward flow of sodium ions followed by a slower recovery to the resting condition lead by a slow flow of potassium ions moving from the inside to the outside of the cell. An AP originates from a stimulus, but the energy for the propagation does not come from the stimulus itself, indeed it is natively stored in the concentration difference that at the resting condition characterizes the membrane as described in the previous sections. Figure 2.8 shows a diagram of an AP with different phases. The resting V_m can actually vary for different cell types, a common value often measured is -60 mV. When the AP is stimulated, sodium channels open very fast and Na^+ ions enter the cell quickly. A recovery phase follows during which potassium ions K^+ exit the cell. During this phase a hyperpolarization may occur that is slower to recover.

Figure 2.9 shows a typical experimental setup to stimulate an action potential. A current or voltage pulse generator is connected to one end of a nerve, while the other end is connected to an oscilloscope for recording the activity generated far away from the stimulus. If the stimulation pulse can vary in amplitude interesting phenomena can be

observed at different amplitudes. The action potential is neither linear nor is it proportional to the stimulation voltage. This section summarizes a few properties characteristic of all electrically active cells.

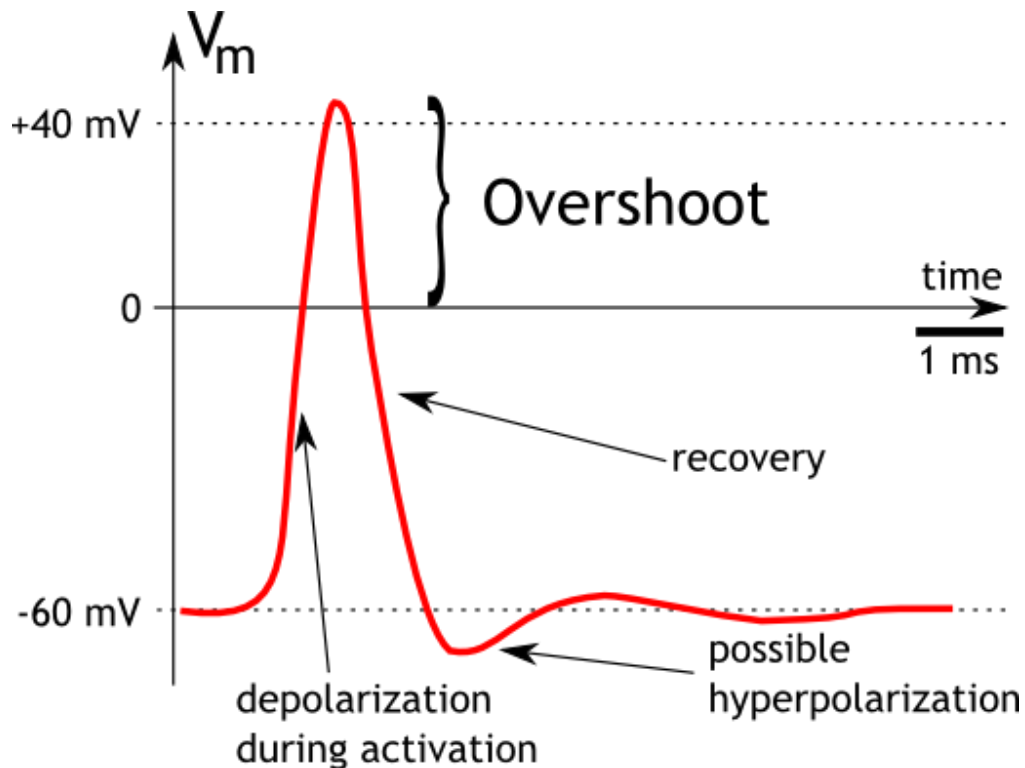


Figure 2.8 Diagram of an AP, with the depolarization phase followed by a recovery phase. Numerical values vary with cell type but values shown are typical.

2.6.1 Stimulation Threshold Voltage

Applying a stimulation pulse such as in Figure 2.9, we could observe that until the pulse reaches a specific threshold value (top two traces in Figure 2.10), at the other end of the nerve a waveform very similar to a passive RC circuit response is observed. When the pulse reaches a certain amplitude (i.e., third trace) an AP can be recorded at the other end of the nerve. Once the threshold is reached, further increases in the applied pulse amplitude do not change notably the observed pulse waveform and amplitude. This is

because the APs are generated before this point in the stimulation and additional stimulation amplitude is thus irrelevant.

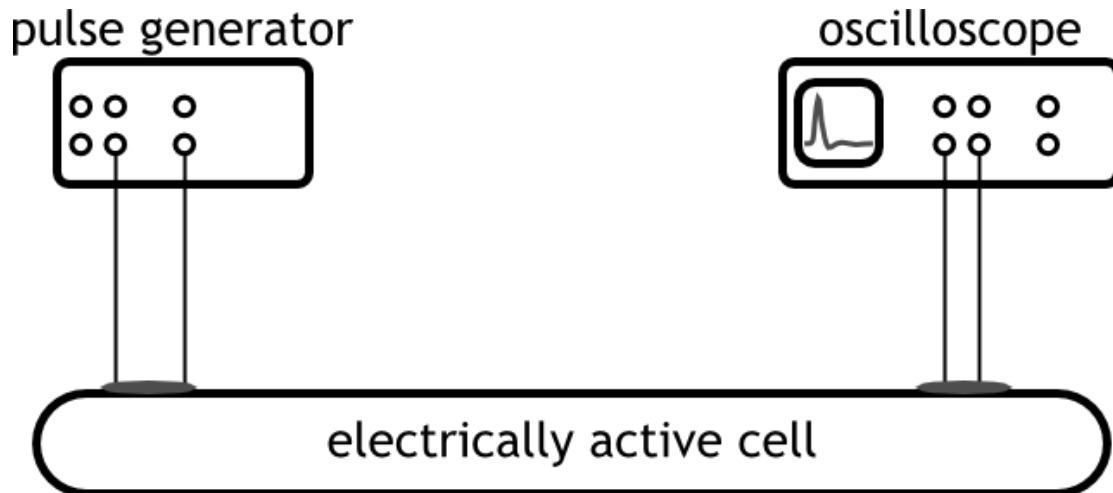


Figure 2.9 A simple experimental setup for recording of an AP. A pulse generator (either voltage or current) is connected at one end of an electrically active cell or fiber. At the other end is connected an oscilloscope for recording the effect generated by a stimulation pulse at a different location. One of the first fibers used in this kind of experiment was the giant fiber of the nerve cord in an earthworm, which consists of an ensemble of electrically active cells.

2.6.2 Other Important Parameters

The threshold level for a nerve fiber or a cell is inversely proportional to the square root of the fiber diameter, i.e. larger cells are stimulated at lower threshold level of the stimulus. The speed of propagation of an action potential is proportional to the square root of the diameter of the cell or the fiber, i.e. an AP propagates faster in a larger nerve.

This difference in speed of propagation within the neural tissue has important implications, especially in fibers composed of a large number of different neural cells, often slightly different from each other. An identical action potential generated at one end of the fiber can result in different copies of the same single action potential recorded

far away from the stimulation site. This behavior has to be taken into account when developing spike sorting algorithms in the FPGA or off line that can easily detect false spikes.

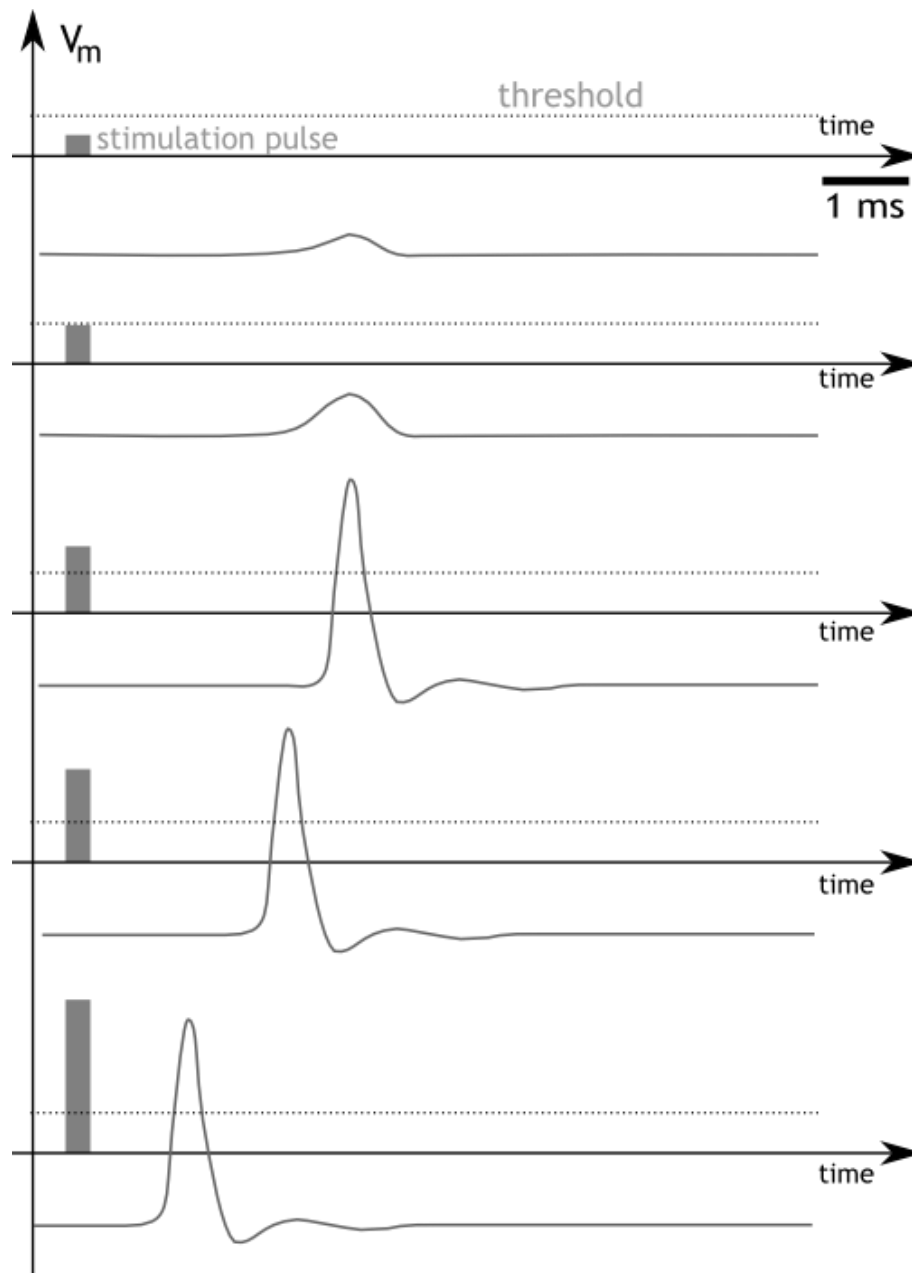


Figure 2.10 A diagram of stimulated electrical activity following a stimulation pulse. Image is not in scale and is not a measure of real action potentials.

2.7 Recording Action Potentials

Over the course of the last decades many successful attempts have been reported for recording and stimulating neural activity from neural tissue or cells by means of electronic devices. The design of such devices is a challenging task because of the reduced strength of the signals themselves and because of the high SNR that such systems require.

A major difference when referring to the AP is the one that exists between the *intracellular action potential* and the *extracellular action potential*. From the physical point of view, they are the same thing: neural tissue is stimulated in some way and the potential energy stored in the difference of ion concentrations through the membrane arises to the propagation along the membrane of the action potential. But from the recording point of view they are very different. In [30], [31], [32] are described two main methods devoted to intracellular recording (*patch clamping*) and extracellular recording (*micro electrode arrays - MEA*). In the first case, an electrode must be placed inside the membrane, while the other electrode acts as the return path of the signal (we discussed this technique in the sections above). In the second case the neural tissue is placed on an array of electrodes (i.e., on an MEA) and the recording consists of a ionic movement a spatio-temporal variation of ionic concentration, i.e. potential, in close proximity to the external part of the membrane. In this case we are then talking of an indirect measurement of the AP.

Figure 2.11 shows a schematic representation of an experimental setup for *MEA* recording. Neural tissue is placed in an electrolytic solution that simulates the natural environment of a cell. On the bottom the neural tissue is in close proximity, but not

necessary in direct contact, with an array of up to thousands of micro electrodes, with dimensions often as low as a few micrometers.

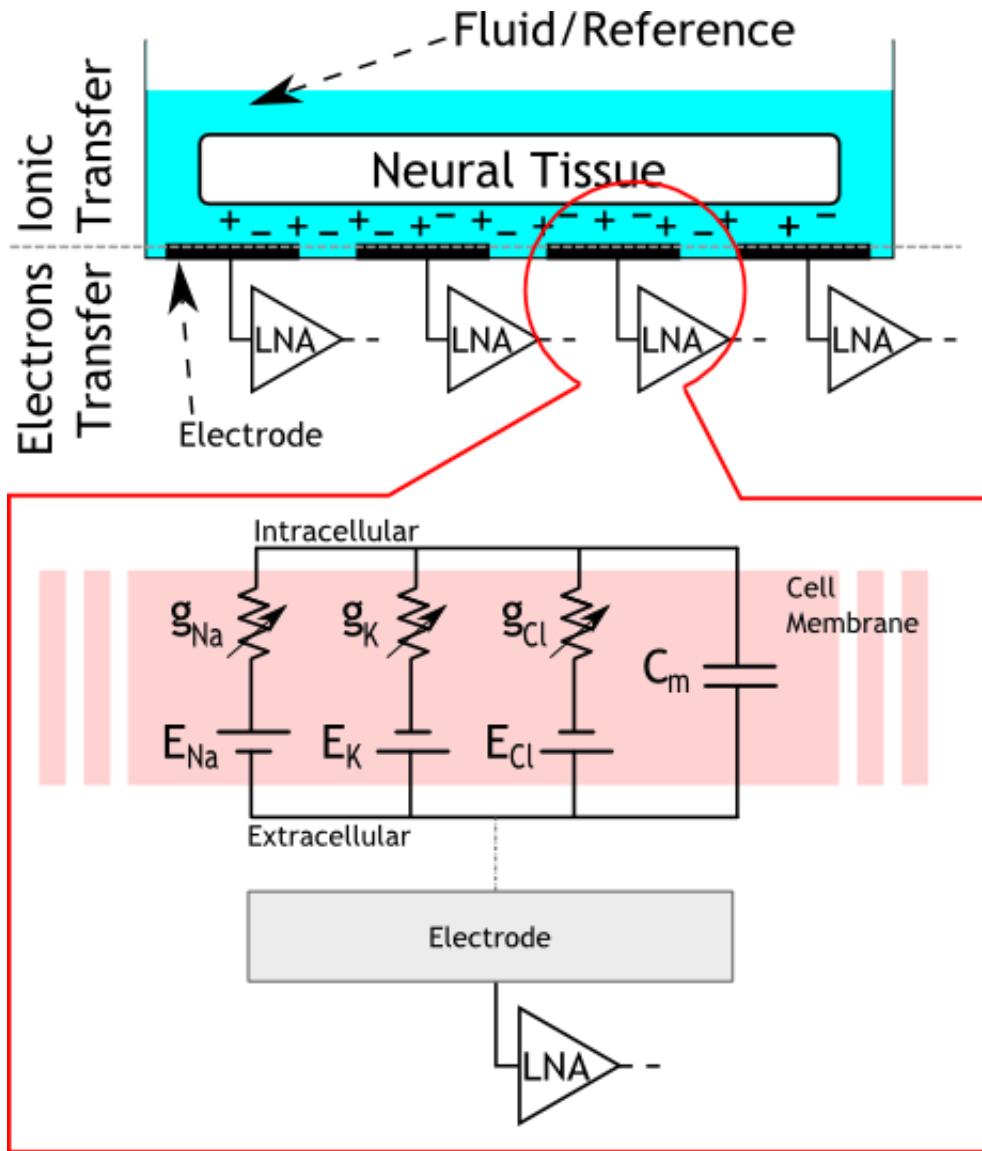


Figure 2.11 A schematic representation of a typical MEA setup where neural tissue lays atop an array of micro-electrodes. The electrodes are connected to a low noise amplifier (LNA) that can be placed *in-situ* to reduce the noise interference of the system.

The electrodes are connected to a low noise amplifier (LNA) amplifier that amplifies and filters the signal recorded with a particular attention for noise. The *LNA* can

be placed in close proximity (for integrated circuit MEAs) or *off-chip* for discrete component systems.

When an AP propagates, the electrode senses the charge unbalance due to the ion movement associated with the action potential itself. Typically such extracellular signals can be as much as three orders of magnitude lower than the typical intracellular response [33].

The main advantage of MEA techniques is that the number of electrodes can be notably larger compared to the patch clamp approach. This characteristic makes this technique useful in cases when a large number of cells, or a distributed system, is to be analyzed. Given the typical dimension of a neuron that can be as low as 10 μm , such an MEA approach could lead to the recording of single cell activity, with a huge impact on the study of the dynamics of large cells populations. Our study is focused on the MEA approach for extracellular recording with the electronics packaged off-chip for development purposes.

Many different architectures have been proposed to address the challenge of reading neural signals when both a very low noise profile and high signal gain are both required. The most interesting and crucial part of a MEA recording electronic system is the first stages of filtering and amplification, the so called *analog front end (AFE)*, that has to maximize the SNR for the system. In the literature many different approaches have been proposed, each of these with advantages and disadvantages, some suitable for *on-chip* integration, some for *off-chip* realization using off-the-shelf commercially available devices. In this section is presented a review of the most common approaches considered while designing the AFE.

2.7.1 Passive High Pass Filter Input

In [23],[34] every electrode El_i is AC coupled by means of a capacitor to an input preamplifier (Figure 2.12). This prevents a low frequency voltage offset shift that may occur at the electrode tissue interface when the signal is amplified. The system features a unity gain high pass filter and low pass filter with a gain of 100 V/V at low frequencies.

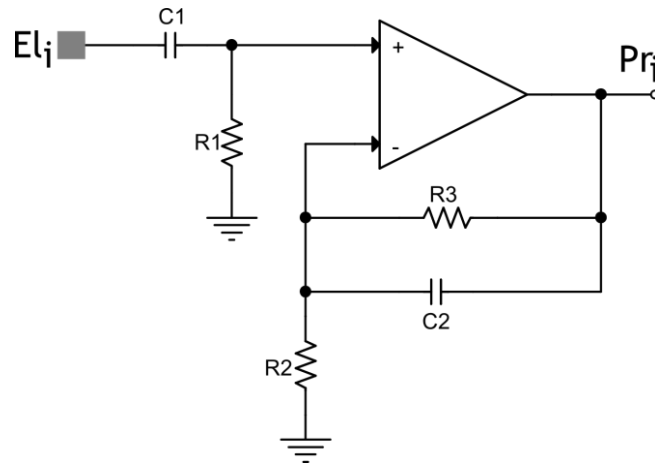


Figure 2.12 The single-ended input low pass filter and preamplification stage is directly connected to the recording electrode.

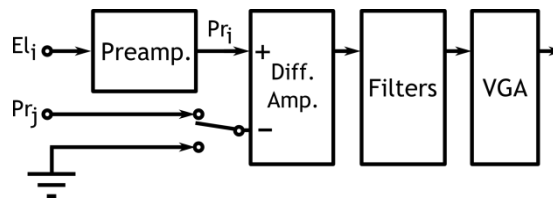


Figure 2.13 A schematic view of the Obeid architecture [23]. The negative terminal of the differential amplifier can be selectively connected to the reference voltage of the fluid or to the output of another channel's preamplification stage.

At the preamplification stage the input El_i is single-ended with respect to the fluid potential. The signal then goes to the inverting input of a differential amplifier with a gain of 10 V/V and a high pass pole. The particularity of this architecture is that the non-inverting input of the amplifier can either be the connections to the reference fluid

voltage or the output Pr_j of another preamplifier to improve signal artifact suppression (Figure 2.13). This feature is especially useful for *in-vivo* applications where artifacts from other activities could lead to false spike detections. In particular the authors were able to cancel undesired mastication noise from recording tracks selecting as the reference an electrode nearby the one under investigation [23].

Following the differential stage the signal enters an additional filtering stage that features three Sallen-Key filters, one high pass and two low pass to reduce the bandwidth of the system, thus reducing the overall Johnson noise propagated down the chain. The last stage is a *variable gain amplifier (VGA)* that adds extra gain (between 1 and 16.5) to the channel for a total gain of 70 to 94 dB.

Table 2.2 lists a summary of the main electrical characteristics of interest for this architecture. The remarkable characteristic of this configuration is the very low input referred noise that prevents the system from complete saturation when larger gains are applied. Moreover, the reference voltage for each channel can be chosen between either the fluid's reference voltage or any other electrode. This reference selection is made after the first stage of preamplification when most of the SNR performance of a circuit is concentrated, thus the typically noisy digitally controlled multiplexer is placed only after this stage, when the signal is already amplified and partially filtered. In order to prevent the input preamplification stage from saturating because of the low frequency varying field potentials at the tissue-electrode interface, the input high pass filter has to be properly designed and the low cutoff frequency must be moved far away from the few hertz domain.

Table 2.2 A summary of the electrical characteristics from the high pass filter input architecture

<i>System property</i>	<i>Value</i>
<i>Gain</i>	70 to 94 dB programmable
<i>High pass cutoff frequency</i>	445 Hz
<i>Low pass cutoff frequency</i>	6.6 kHz
<i>Input referred noise</i>	1 μV_{RMS}
<i>Integrated Circuit</i>	No
<i>Stimulation capable</i>	No

2.7.2 Capacitive Inverting Input

In [35]-[38] the input high pass filter is embedded in the preamplifier which consists of an inverting capacitive operational amplifier configuration. The system is realized as an *application specific integrated circuit (ASIC)*. Figure 2.14 shows the schematic diagram of preamplifier and the analog multiplexers used to connect different electrodes in *time domain multiplexing (TDM)* to reduce the number of preamplification channels as the number of electrodes increases. The input capacitance C_1 provides a high impedance path for low frequencies and a zero DC biasing current for the circuit.

The gain of the first stage of amplification follows the relation

$$G = \frac{-R_{NMOS}C_1}{1/j\omega + R_{NMOS}C_2} \quad (2.32)$$

which for high frequencies can be reduced to $-C_1/C_2$. The low corner frequency of this high pass circuit depends on the capacitor and resistor values. In particular, for the low corner frequency the resistance must be very high and high-resistance sub-threshold

biased MOSFETs are used to achieve a $15.9 \text{ G}\Omega$ value. This value is adjustable by varying the gate polarization voltage of the MOSFETs and this characteristic makes the system very flexible and suitable for different experiments; a low corner frequency can be set very low to read field potentials on the order of a few hertz, or high to reduce the low frequency Flicker noise of active devices. This high pass corner frequency varies among the different papers from 66 mHz to 100 Hz. The low pass corner frequency is mainly due to the amplifier internal intrinsic pole and is 24 kHz. The system features an overall gain of 40 dB in the band considered with an input referred noise for the amplifier stage of $16.6 \mu\text{V}_{\text{RMS}}$ integrated between 100 Hz and 10 kHz when the input multiplexer is not considered. The input selection 64 x 8 multiplexer gives a huge advantage in terms of spatial occupation because this helps by reducing the area required by a factor 1:8. But this multiplexing is performed before the first stage of amplification and this characteristic partially degrades the input referred noise figure, which increases up to $19.2 \mu\text{V}_{\text{RMS}}$ considering also the frontend selection stage [35].

The channel input is single ended and the circuit reference is the fluid reference voltage. The eight different lines from the respective preamplifiers are further time domain multiplexed to a single line that includes all 64 channels. An additional gain of 20 dB is provided before reading out the stream with an ADC.

The power consumption for the single channel is predicted to be $92 \mu\text{W}$ assuming $\pm 1.5 \text{ V}$ supplies. The predicted power consumption for the whole system, including the analog front-end selector and the complementary stages of amplification, is $8314 \mu\text{W}$.

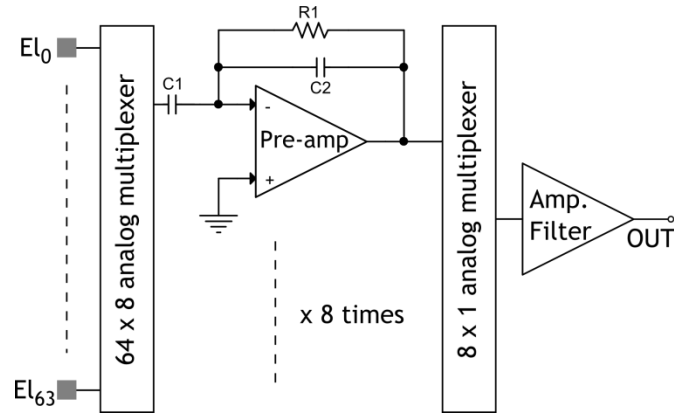


Figure 2.14 The input circuit of the Olsson/Wise architecture where the gain is obtained as $-C_1/C_2$. $C_1 = 10$ pF, $C_2 = 0.1$ pF for a nominal fixed gain value of 100.

From an architectural point of view it is interesting how this architecture integrates a digitally controlled analog multiplexer before the preamplification stage without dramatically compromising the noise performance of the circuit. This is an important factor as the number of electrodes scales out to hundreds or even thousands. The main limitation introduced by this higher input referred noise parameter is the maximum full chain gain that can be provided before the output is completely unreadable because of the noise. A simple calculation based on $20 \mu\text{V}_{\text{RMS}}$ noise at the ± 1.5 V of power supply is that the maximum gain to obtain a signal to noise ratio of at least 5 is

$$G = \frac{1.5/\sqrt{2}}{20 \cdot 10^{-6} \cdot 5} \cong 10\,600. \quad (2.33)$$

which can be a limiting value for certain experiments.

Table 2.3 provides a summary of the most important electrical characteristics of this architecture with the tunable high pass, low corner frequency by means of subthreshold MOSFETs based resistors.

Table 2.3 A summary of the predicted electrical characteristics from the capacitive inverting input architecture.

<i>System property</i>	<i>Value</i>
<i>Gain</i>	60 dB theoretical (58.2 measured)
<i>High pass cutoff frequency</i>	66 mHz to 100 Hz
<i>Low pass cutoff frequency</i>	24 kHz
<i>Input referred noise</i>	19.2 μV_{RMS}
<i>Integrated Circuit</i>	Yes
<i>Stimulation capable</i>	Yes/No

2.7.3 Differential Capacitive Input

In [33] and [39] a 128 electrode integrated differential capacitively coupled input stage is presented that is based on an *operational transconductance amplifier* (OTA).

Figure 2.15 shows the basic architecture of the capacitive input differential approach. The electrode El_0 is the main electrode while the reference electrode El_{REF} can presumably be any other electrode from the 128 electrode array, but it should be noted that this point is not clear from the literature. R_1 and R_2 are still realized as tunable sub-threshold MOSFETs due to the high values necessary to obtain a low cutoff frequency for the high pass amplifier. The preamplifier supplies a gain of 20 dB to the signal from the electrode, which is then low pass filtered with a unity gain passive component based filter, and then further amplified with an additional 30 dB of gain. The signal is then time domain multiplexed by means of an eight to one analog multiplexer and, finally, an additional 10 to 20 dB of amplification are provided to the TDM waveform for a total maximum gain of 70 dB.

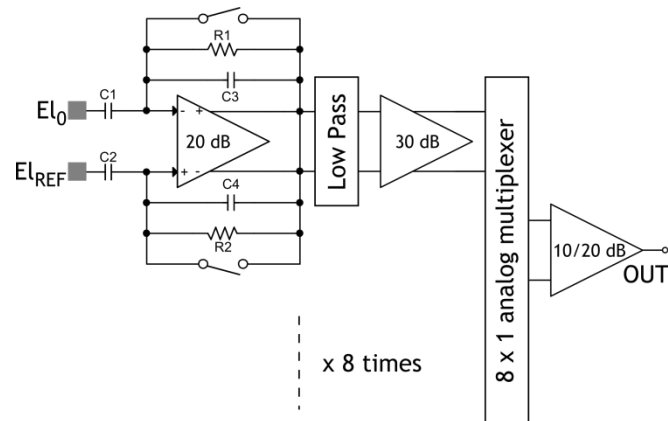


Figure 2.15 The recording front end of the capacitive input differential architecture. The resistors R_1 and R_2 are made out of MOS resistors to obtain very high values required to set the high pass corner frequency to a few Hz.

This architecture features pulse artifact removal capabilities. Voltage pulses used to stimulate neural activity are normally very large compared to the AP signals the AFE normally record. They can go for a few volts [40] up to 50/100 V [41]. These voltage levels are an order of magnitude larger than the input signals to be read, and when they appear at the AFE input they can easily saturate the input of successive amplification stages. Typically time constants of such a circuit are slow in order to be able to amplify low frequencies as well as high frequencies. This characteristic results in long recovery times of the amplification chain from the stimulation pulse appearance to the moment it is ready to properly record the stimulated activity. This figure is clearly not suitable when we want to record stimulated APs which may occur hundreds of microseconds after the stimulation pulse.

The authors of these works proposed a solution to this problem that consists of two digitally controlled integrated switches in parallel to R_1 and R_2 . These switches, when closed, i.e. for the entire stimulating pulse duration, place the OTA in the buffer configuration letting the output follow the input with unity gain. The time constant in this

configuration in very fast, mainly dependent on the speed of the OTA and the normal recording conditions after the pulse can be recovered is less than 100 μ s. After the pulse ends, the switches are opened and the circuit and the standard characteristics of the circuit are restored.

The integrated circuit is realized in standard CMOS technology and the reader should refer to the original papers for more details about the device internal circuit diagrams.

Table 2.4 provides a summary of the most important electrical characteristics of this architecture.

2.7.4 Active Pixel Sensor Micro Electrode Array

In [42], [43] the authors report an architecture tailored to read out a large amount of electrodes (4096), that uses an active pixel sensor (APS) approach. A 256 column by 16 row pixel array is scanned row by row, time domain multiplexing the signals coming from the single pixel. The total active area of the sensor is 2.67 mm x 2.67 mm.

The electrode is DC coupled to the gate of a MOS transistor properly biased by a dedicated circuit (Figure 2.16). Changes to the electrode voltage induce a variation on the MOS channel conductance which is reflected at the amplifier input through the biasing circuit.

The first stage of amplification features a 40 dB gain before the signal is sampled and transferred to a variable gain amplifier that can be programmed to have a gain between 12 and 36 dB. The total channel gain is then 52 dB to 76 dB. The desired number of columns is time domain multiplexed to form the row data. The electrodes are divided into 16 rows of 256 columns each, but due to switching noise and issues with the

full bandwidth of the multiplexed signal only 16 columns are read during each cycle to preserve a low noise condition [42].

Table 2.4 A summary of the electrical characteristics from the differential capacitive input architecture.

<i>System property</i>	<i>Value</i>
<i>Gain</i>	60 or 70 dB
<i>High pass cutoff frequency</i>	1 Hz to 1 kHz
<i>Low pass cutoff frequency</i>	1 to 30/50 kHz
<i>Input referred noise</i>	11.7 μV_{RMS} between 100 mHz - 100 kHz
<i>Integrated Circuit</i>	Yes
<i>Stimulation capable</i>	Yes

Isolating the DC component of the neural signal while being able to record low frequencies that arise, for example, from the field potentials at the tissue electrode interface requires the use of a very large capacitance at the input stage. When the number of recording sites increases the space available for the single *in-pixel* read-out circuitry is lower and lower. Space was the main concern for the authors of this system and to overcome this limitation they proposed this original configuration where an autozeroing circuit was used to both calibrate and bias the input MOSFET during recording. The required calibration phase does not typically require more than 1-2 s.

For a single channel during static operation, i.e. no switching between columns and rows occurs, the system features an 11 μV_{RMS} input referred noise measured with a gain of 55 dB for a bandwidth of 5 kHz. When in dynamic operation, the row and column

selection circuit switches introduce an additional commutation noise bringing the input referred noise to $26 \mu\text{V}_{\text{RMS}}$.

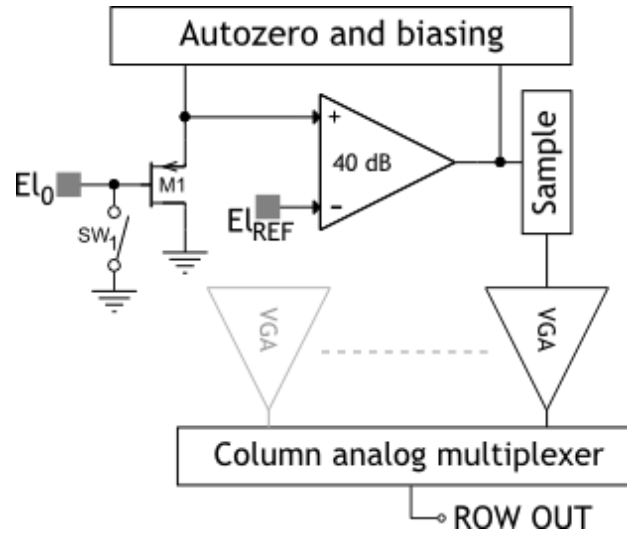


Figure 2.16 A schematic representation of the circuit. SW1 is part of the auto-zeroing circuit necessary because of the DC coupling of the input electrode to the amplifying circuitry.

Table 2.5 summarizes the main electrical characteristics of the Active Pixel Sensor Micro Electrode Array architecture.

2.7.5 Recording Unit with Active Stimulation Artifact Compensation

In [44] and [45] the authors propose a system realized using off-the-shelf components (Figure 2.17). The most remarkable feature of this system is an original method to resolve the problem of avoiding saturation after a stimulation pulse artifact. As explained above, stimulation pulses can be order of magnitudes larger than the neural signals. When this pulse reaches the amplification circuit it causes the whole chain to saturate and, as explained above, it can lead to very long recovery times after stimulation before the filters and the amplifier can recover to the natural resting condition for which they are designed.

Table 2.5 A summary of the electrical characteristics from the active Pixel Sensor Micro Electrode Array.

<i>System property</i>	<i>Value</i>
<i>Gain</i>	52 to 76 dB
<i>High pass cutoff frequency</i>	Unknown
<i>Low pass cutoff frequency</i>	5 kHz
<i>Input referred noise</i>	11 μV_{RMS} static 26 μV_{RMS} dynamic
<i>Integrated Circuit</i>	Yes
<i>Stimulation capable</i>	No

When recording the stimulation line is disconnected from the electrode by opening switch SW_{stim} and SW_{add} , while $SW_{s/h}$ is kept closed. The signal flows through the preamplifier (with gain of 20 V/V) and the main amplifier with gain of 500 V/V.

During the stimulation pulse $SW_{s/h}$ is opened and the last value of the preamplifier output is stored at the feedback amplifier thanks to a capacitor. This value is attenuated by a factor of 20 V/V (the same gain as the preamplifier stage) and it is added to the actual stimulation waveform coming from the stimulation circuitry. The resulting waveform has the same shape of the stimulation pulse but presents an offset equal to the electrode voltage an instant before the system passes from recording to stimulation mode. Once the stimulation waveform ends, $SW_{s/h}$ is closed while SW_{stim} and SW_{add} are opened. At this point in time the preamplifier input is the value that it was just before the stimulation pulse and, theoretically, this would filter signal artifacts and prevents the system from saturation. This solution shows a fast recovery time just after stimulation.

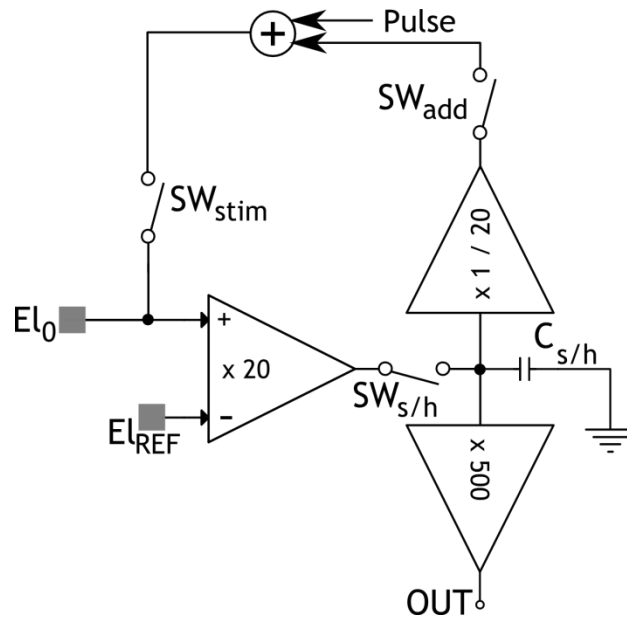


Figure 2.17 The circuit diagram with both the amplification circuitry and the active stimulus artifact compensation system.

The total gain is 80 dB in a band between 100 Hz and 10 kHz, with a peak-to-peak input referred noise of 10-20 μV_{PP} , i.e. 7-14 μV_{RMS} .

Table 2.6 summarizes the main electrical characteristics of the recording unit with active stimulation artifact compensation.

2.7.6 OSFET Input Stage

In [46]-[50] the authors propose a very interesting method for recording neural activity from extracellular MEAs which is based on an active electrode built from an oxide-semiconductor field effect transistor (OSFET).

The basic idea [49] is that the conductive media in which the cell is immersed acts the conductive gate region of a virtual MOSFET device. The bulk material in which the electrode is fabricated is insulated from the electrolytic fluid by means of an insulating layer. The pMOS transistor *MI* in Figure 2.18 is biased at a certain value of drain and

source gain in such a way that the biasing current I_{SD} is in the resting condition, i.e. no AP occurs, is 300-400 μA on a resistor R_I of 10.8 k Ω .

Table 2.6 A summary of the electrical characteristics from the recording unit with active stimulation artifact compensation.

<i>System property</i>	<i>Value</i>
<i>Gain</i>	80 dB
<i>High pass cutoff frequency</i>	100 Hz
<i>Low pass cutoff frequency</i>	10 kHz
<i>Input referred noise</i>	7-14 μV_{RMS}
<i>Integrated Circuit</i>	No
<i>Stimulation capable</i>	Yes

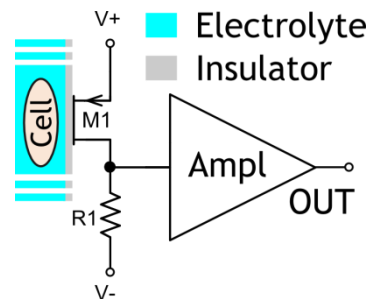


Figure 2.18 The basic circuit diagram of the OSFET electrode approach.

A 10 mV voltage change on the electrolyte side causes a source-drain current variation of $-1 \mu\text{A}$, giving an almost unity gain. The signal then goes through an amplification and filtering stage to achieve the desired gain and to limit the bandwidth of the noise.

This approach has been used in [50] as the *in-situ* electrode analog signal conditioning to build a 128 by 128 electrode array which is, based on a thorough review

of the literature, the largest number of electrodes successfully assembled in a single chip with *in-situ* recording and signal conditioning capabilities. The solution adopted in this case is much more complex but the basic architecture remains the same.

The authors in this case are more interested in pulse sorting rather than the precise frequency response of the amplifying chain. In [49] appears the first successful achievement of a real time communication between two neurons not in contact to each other.

Neurons (A) and (B) from Figure 2.19 are not connected and, theoretically, the activities of the two cells are uncorrelated. When an AP is spontaneously fired by (A) the system detects it through (C). The fact that some neural activity has occurred on (A) is acknowledged to the stimulation unit (D) via a delay line and at that point (D) generates stimulation pulses to activate (B). This study represents a huge step forward in rehabilitation engineering after, for example, a trauma at the spinal cord interrupts a neural pathway and the nerves are not able to communicate with each other anymore. Table 2.7 shows a summary of the main electrical characteristics for the system.

2.8 Summary

In this chapter I first described the theory behind the signal propagation within the human body, by means of action potentials. The generation and propagation of such electrical activity has been taken into account and both a qualitative and a quantitative model of the membrane have been presented. A comprehension of the mechanisms behind the action potentials is necessary to understand the importance of the limiting values typical of electronic system thought to acquire and to stimulate such activity.

The second part of the chapter focuses on different architectural approaches used in the past to acquire action potentials. For each architecture we described the general idea focusing on the first stage of amplification that is typically the most important from a point of view of noise of the system, impedance and bandwidth.

These characteristics have been tabled for easy comparison, with one of them, the passive high pass input front end over performing the other approaches on the input referred noise figure.

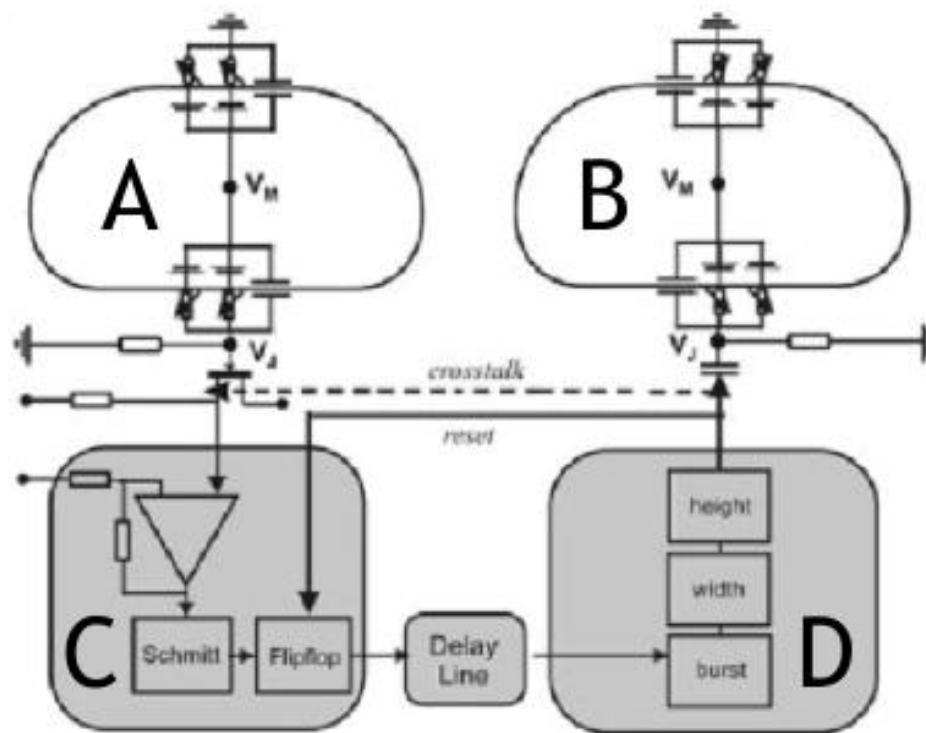


Figure 2.19 The schematic diagram of the experiment for reconnection of two separates neurons (A and B). C is the recording system that sorts the AP and passes it to the stimulation circuit while D stimulates an AP on the receiving neuron (B).

Table 2.7 A summary of the electrical characteristics from the OSFET input stage architecture.

<i>System property</i>	<i>Value</i>
<i>Gain</i>	84 dB
<i>High pass cutoff frequency</i>	Unknown
<i>Low pass cutoff frequency</i>	Unknown
<i>Input referred noise</i>	Unknown
<i>Integrated Circuit</i>	Yes
<i>Stimulation capable</i>	Yes

CHAPTER 3: DESIGN AND PROTOTYPING OF A CUSTOM BRAIN COMPUTER INTERFACE

In this chapter a custom architecture will be presented based on specifications related to experiments recently conducted by Dr. C. L. Frewin of the USF SiC group. The architecture has been designed, simulated, realized on a PCB board, electrically tested and used to both stimulate and record actual neural activity for validation. The system specifications were challenging compared to other systems both from the literature and those that are commercially available, and the realization of such a system involved many fields of research, from accurate analog design to minimize noise during recording, to a complex control system based on a *field programmable gates array (FPGA)* development board to control the functioning of all the units together and the transfer of a huge amount of recorded data to a persistent storage like a PC.

In the next sections we will go through the system specifications, the global architecture, the single unit circuits, the FPGA firmware that controls the whole system and realizes a first stage of digital filtering, and finally the custom Java software written to acquire and store the massive amount of data from the future full system made of up to 64 channel of recording.

3.1 Motivation and System Specifications

All of the different architectures found in the literature and presented in the previous chapter are different in many aspects from each other, but they also have one common characteristic that limits their field of use - they are all designed for low voltage

systems, where the recorded signals are typically 5 mV maximum and the stimulation pulses that the analog front end (AFE) has to withstand rarely exceed a few volts. Many of the systems described above are realized using standard CMOS fabrication techniques on silicon substrates: this choice allows for the building of the analog signal conditioning electronics *on-board* thus minimizing the external noise invasiveness that would result from long connection lines. Silicon CMOS processes are also cheap and this would make this material a perfect candidate for implantable smart medical devices. Unfortunately, as we demonstrated before in Chapter 1, silicon has been demonstrated to be reactive when exposed in a typical body environment for long time intervals. As new materials, like silicon carbide, are used to realize electrodes and substrates for this circuitry a very flexible system is required to stimulate and record neural activity with these new electrodes. As a matter of fact different materials can present remarkably different electrical characteristics, required very high noise figures and gain to read out signals from electrodes realized with such materials.

3.1.1 Specifications for Noise, Gain and Bandwidth

A typical extracellular action potential recording has an amplitude at the electrode typically between 30 μ V and 2 mV and in a frequency range with most of the frequency content that between a few hertz up to 10 kHz [39]. A minimum *signal to noise ratio* (SNR) value considered acceptable for neural recording is 5 [21]. Considering a ± 2.5 V power supply we can easily calculate the gain requirements necessary for such a system. For the minimum gain we have:

$$G_{min} = \frac{2.5V}{2 \cdot 10^{-3}V} = 1250 V/V \cong 62 dB \quad (3.1)$$

while for the maximum gain we have

$$G_{max} = \frac{2.5V}{3 \cdot 10^{-5}V} = 83333 V/V \cong 98 \text{ dB}. \quad (3.2)$$

Based in these considerations we require our system to have a gain that can be set between 62 and 100 dB in a band between 20 Hz and 10 kHz. In order to perform different experiments and measurements there must be the possibility of programming it in real time via a software interface. In order to comply with the noise requirements and, in particular, a SNR of at least 5, we can easily calculate what is the maximum allowed noise that can added by the circuit.

At the maximum gain of 100 dB over a $\pm 2.5 V$ as the analog to digital converter range, we can have a maximum input referred RMS noise, V_{RMS} , of

$$Noise_{input} = \frac{2.5V \cdot 1/\sqrt{2}}{10^5 \cdot 5} = 3.5 \mu V_{RMS}, \quad (3.3)$$

which corresponds to an input noise density $\sigma_{input} = 0.35 \text{ nV}/\sqrt{\text{Hz}}$. This measurement can be performed with the system input short circuited to the reference voltage and will be presented later in this chapter.

3.1.2 Specifications for Stimulation Voltage Pulse Generator

On the stimulation side the system is designed to generate bipolar voltage pulses with positive and negative phase duration of 100 μs (t_1-t_2 and t_3-t_4 in Figure 3.1). The rising and falling edge times of the pulses are fixed to 10 μs for the half step, e.g. t_0 to t_1 , and to 20 μs for the full step from t_2 to t_3 . The standard time between two pulses, called the *resting time*, is by default set to 9.8 ms but can be software programmed to the user's needs.

The maximum pulse amplitude is ± 50 V. Typically voltage pulses used in such experiments are much lower than this [21], that is because for common electrodes materials like gold and titanium higher voltages would cause irreversible effects at the electrode-fluid interface. But in some cases, for example for Intracortical microstimulation (ICMS), relatively high voltages (50-100 V), are required [41]. This requirement means that the low-noise, low-voltage devices must be protected. Consequently this requirement determines the input stage architecture for the AFE.

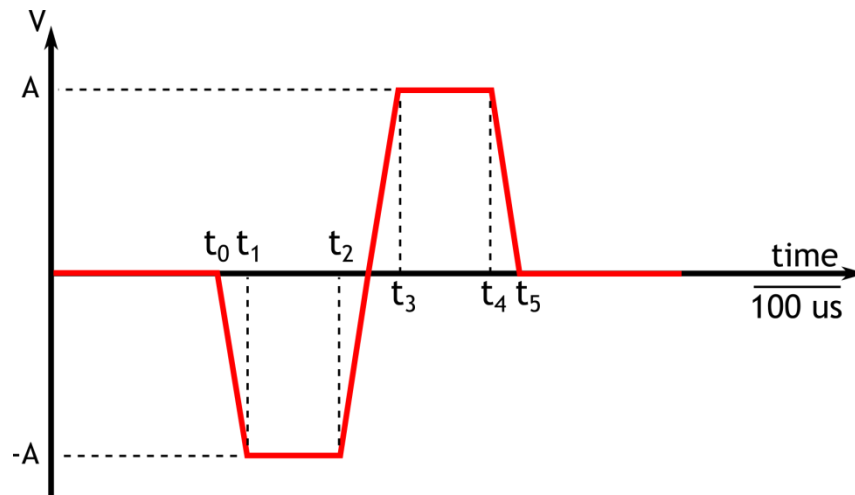


Figure 3.1 Desired stimulation pulse waveform. The pulse amplitude, may vary between 0 V and 'A', the pulse has finite rise and fall times of maximum $10 \mu\text{s}$ (e.g. the t_0 - t_1 interval) and a biphasic phase duration of $100 \mu\text{s}$ (t_1 - t_2 and t_3 - t_4 intervals).

The pulsed stimulation signal must be a differential signal floating with respect to the fluid reference voltage. This specification requires a secondary power supply line for which the reference voltage is not connected to the main reference voltage.

3.1.3 Signal Digitalization and Persistent Storage

The system must be capable of creating a digital copy of the APs recorded from the neural neurons and storing it to a persistent storage unit. A single channel has a bandwidth of 10 kHz, so a sampling frequency of at least 20 ksp/s (kilo samples per

second) must be used. In order to avoid aliasing issues we define our sampling frequency as 1 Msps for 16 channels, which results in 62.5 ksps for the single line. Based on [23] we decided to use a 12 bit ADC for the conversion.

A continuous recording of 64 channels sampled at 62.5 ksps each, using a 12 bit ADC, gives a data flow of

$$\text{Bitrate} = 64 \text{ ch} \cdot 62\,500 \text{ sps} \cdot 12 \text{ bit} = 48 \text{ Mbps} \quad (3.4)$$

which is a massive amount of data flowing from our system to a PC. This value must be interpreted to reduce the bit rate because, in the future, the system will be expanded to feature a larger number of electrodes. This is important since the *bitrate* grows linearly with the number of electrodes in the system.

This data must also be stored on a PC in an accessible data format for further analysis and elaboration. As a first choice we chose to use *comma separated values* (CSV) files but this feature can be easily modified later by rewriting a limited part of the software.

3.1.4 Specifications Summary

Table 3.1 lists all the main system design specifications that we extracted, both from the literature and from the explicit experimental requirements from the SiC group. Some of these are common in the literature, like the low required input referred noise and the system bandwidth, while others are challenging like the high gain (100 dB) and the combination of this high value with very high stimulation pulse amplitudes.

Table 3.1 A summary of the system specifications.

<i>Property</i>	<i>Value</i>	<i>Notes</i>
<i>Gain</i>	62 to 100 dB	Software programmable
<i>Bandwidth</i>	20 Hz to 10 kHz	
<i>Input Referred Noise</i>	$< 3.5 \mu\text{V}_{\text{RMS}}$	With the input connected to ground
<i>Number of Channels</i>	64	Modularized architecture
<i>Stimulation Pulse</i>	Biphasic ± 50 V	Software programmable amplitude down to ± 0.2 mV
<i>Analog Front End</i>	± 50 V	Capable of withstanding high voltages
<i>Channel sampling frequency</i>	62.5 ksps	
<i>Data storage</i>	CVS file	On a PC

3.2 A System Overview

The system is designed to interface with a 64-electrode MEA, but the number of inputs is scalable. The signal from the electrodes (Figure 3.2) goes through an *analog front end (AFE)* to be filtered and amplified. The 64 channels are divided into four (4) 16-channel modules which are identical to each other. This number is scalable and it can be increased without any structural system modification. The 16 channels from each of the 4 recording modules are *time domain multiplexed (TDM)* to a single data line and the output is read by an analog to digital converter (ADC) at a frequency rate of 1 Msps/12 bit for the 16 channel multiplexed line, i.e. 62.5 ksps for each channel as discussed in the last section.

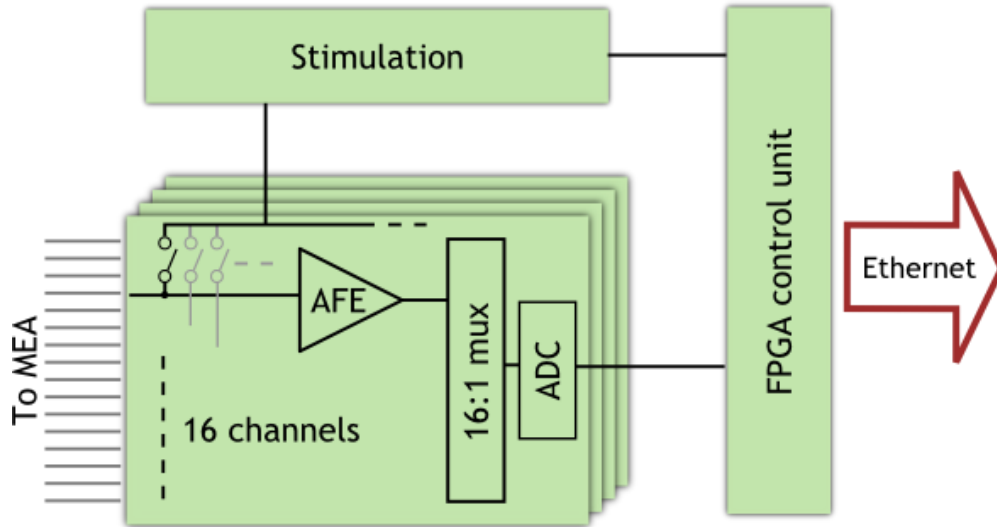


Figure 3.2 A system overview of the whole unit assembly. The three principal circuit blocks are the 16-channel board, the stimulation board and the FPGA control unit board, as shown.

Each of the 4 ADCs from the four (4) 16-channel units is read by the main FPGA control unit and the data sent to a PC via an Ethernet connection for persistent storage.

The Ethernet connection provides bidirectional communication, for both signal acquisition and system control. Experiment parameters like the pulse width and amplitude, or the channel gain, can be controlled remotely via a GUI interface. A custom Java driver has been written to receive data packets from the FPGA and to program the system. During normal recording the stimulation circuit output is disconnected from the electrode lines by means of high-voltage digitally controlled analog switches. These switches, as described below, can be selected to send the stimulation pulse to any electrode of the 64 channels in order provide a high flexibility for stimulation paths.

3.3 System Architecture: Design and Simulation

In this section is a detailed description of the system building blocks, their function and, when applicable, the simulated parameters and characteristics. Figure 3.3 shows a schematic representation of the analog front end featuring the protection circuit directly connected to the MEA electrodes, the low noise amplifier, the Sallen & Key low pass filter, the digitally controlled low noise amplifier, and the data conversion module with the 16 to 1 analog multiplexer and the analog to digital converter for data sampling.

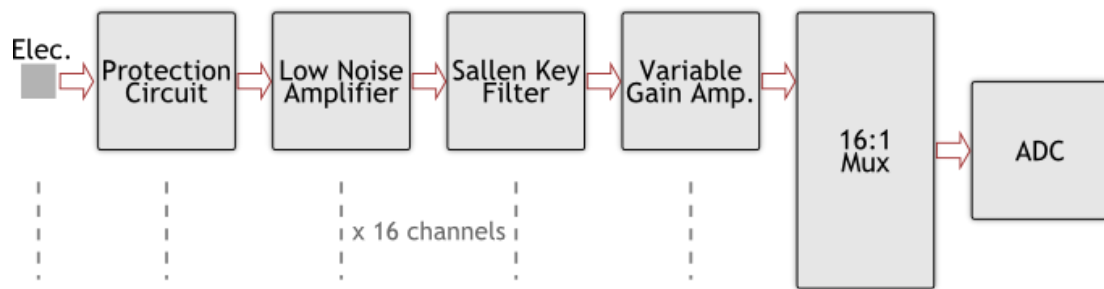


Figure 3.3 A block diagram representation of the AFE unit for signal recording showing, in order: the electrode, the protection circuit, the low noise amplifier, the Sallen & Key filter, the variable gain amplifier, the multiplexer and the analog to digital converter.

3.3.1 The Protection Circuit

The protection circuit is the first interface between the electrode and the electronics system and the main functions of this module are as follows: to increase the input impedance seen from the electrode in both recording and stimulation mode, to act like a unity gain voltage amplifier for the small signals from the electrode, i.e. the APs, to provide a large current amplification during pulses to charge the capacitance at the low noise amplifier input without sinking that current from the electrode and the stimulation circuit (Figure 3.4). Figure 3.5 shows the schematic for the protection circuit that consists of a Darlington BJTs unity gain input stage.

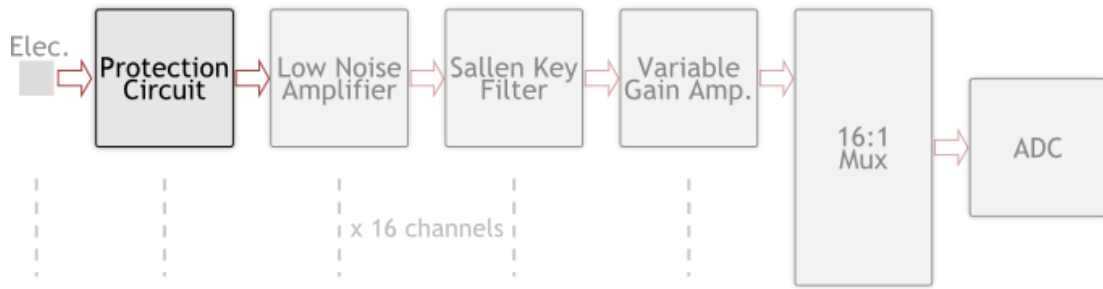


Figure 3.4 The protection circuit: the first interface to the electrode.

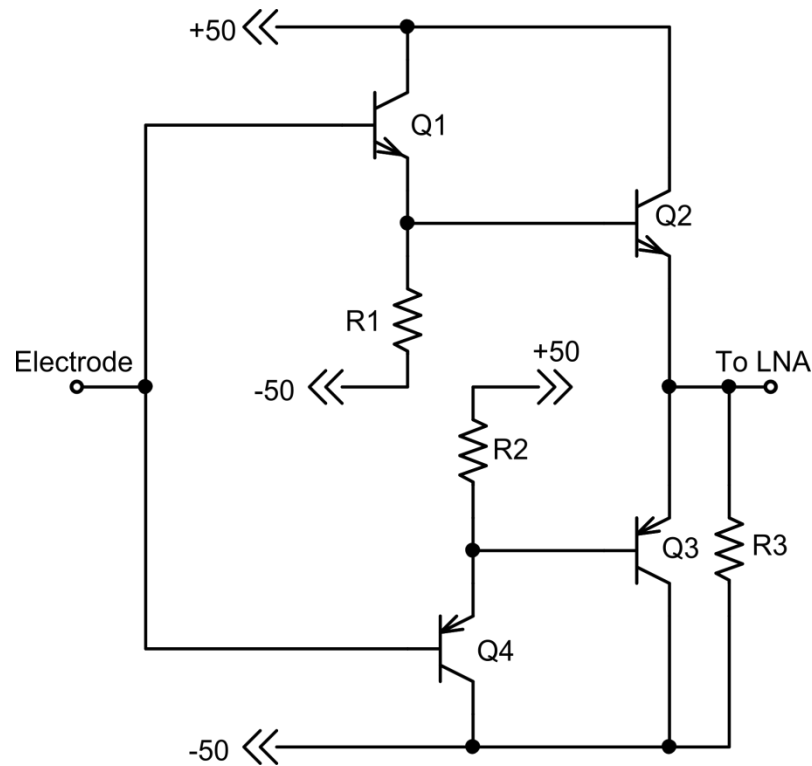


Figure 3.5. The schematic circuit of the protection block. R_1 and R_2 are $5.6\text{ M}\Omega$ resistors that provide a path to switch off the second transistor of the Darlington configuration. R_3 ($220\text{ k}\Omega$) provides a path for the biasing current from Q_2 .

When in recording mode the Q_2 emitter terminal follows the input electrode voltage with a dc offset that results from the base-emitter voltages of Q_1 and Q_2 (model PBSS305ND, NXP Semiconductors) thus $V_{out} = V_{BE1} - V_{BE2}$. This voltage drop

corresponds to about 0.9 V. During this phase the negative branch of the circuit Q_3 and Q_4 (model PBSS305PD, NXP Semiconductors) is switched off. Thus the configuration realizes a unity voltage gain amplifier.

The biasing current in this phase is $I_{R6} = 50V/220\text{ k}\Omega \cong 230\mu A$. For collector current the BJTs used supply an extremely high value of h_{FE} larger than 300. Thanks to the Darlington configuration, the input biasing current is then reduced by a factor larger than 90,000 to a few picoamperes.

During stimulation the circuit behaves once again as a voltage follower. During the falling edge interval between t_0 and t_1 (Figure 3.1) the input electrode is driven toward the most negative voltage, e.g. -50 V, from the stimulation circuit. The upper branch of the protection circuit is off because V_{BE1} and V_{BE2} tend to be negative. Instead the negative part of the circuit, formed from Q_3 and Q_4 , is on and drives the output toward negative voltages following the input. During the rising edge of the pulse, i.e. the t_2 to t_3 interval, the negative branch of the circuit tends to be off, while the upper positive part drives the signal toward positive voltages. Note that in this case all of the current necessary to charge the downstream capacitances is provided by the protection circuit itself through the Q_2 collector terminal. During the interval t_4 to t_5 we have exactly the same conditions described above with the lower circuit branch driving the signal.

These features are very important from an electrical point of view. The downstream high pass filter and amplifier (Figure 3.6) presents at the input a high pass capacitor and the amplifier features internal protection diodes that prevent the input voltage of the amplifier to change beyond ± 2.5 V (the supply voltage of the amplification stage). During the stimulation pulse edge, e.g. the positive swing during t_2 and t_3 , the Q_1

base, and consequently Q_2 emitter, are driven toward +50 V by the stimulation circuit. When the LNA protection diode turns on a large current is required to charge C_1 up to +50 V. On the right side the current is provided by the diode, on the left side it would have been provided, if the protection circuit was not present, by the stimulation circuit. Therefore the presence of the protection circuit reduces notably the current required by a factor 10^5 . In fact, the current to charge C_1 is provided by the collector of Q_2 instead of the stimulation circuit. This feature is extremely useful because in many cases the stimulation pulses are controlled in current with values of not more than a few milliamperes [21].

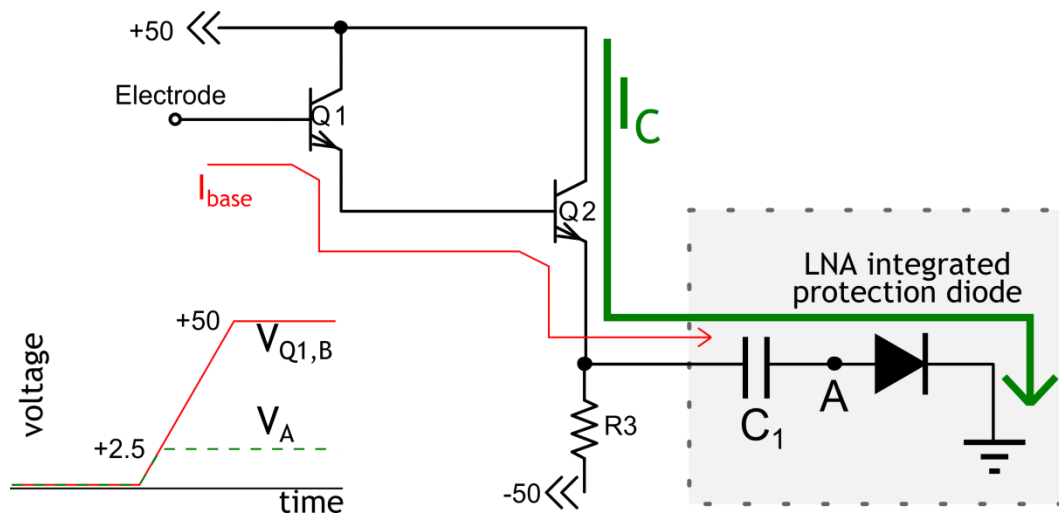


Figure 3.6 The current path through the protection circuit during a positive stimulation pulse. Once the protection diode turns on, the voltage V_A is kept constant at about 2.5 V, while the electrode tends to rise to +50 V. In this case the protection circuit provides the current I_C to charge the capacitor while the current I_{base} from the stimulation circuit is 10^5 times lower.

3.3.2 The Low Noise Amplifier

After the protection circuit the signal from the electrode goes through the first stage of amplification, the low noise amplifier (LNA) shown in Figure 3.7. At this point the signal has not been amplified or filtered and the signal conditioning at this stage is

very important and will determine the most important performance requirement, the input referred noise of the system. Figure 3.7 shows the LNA analog conditioning chain.

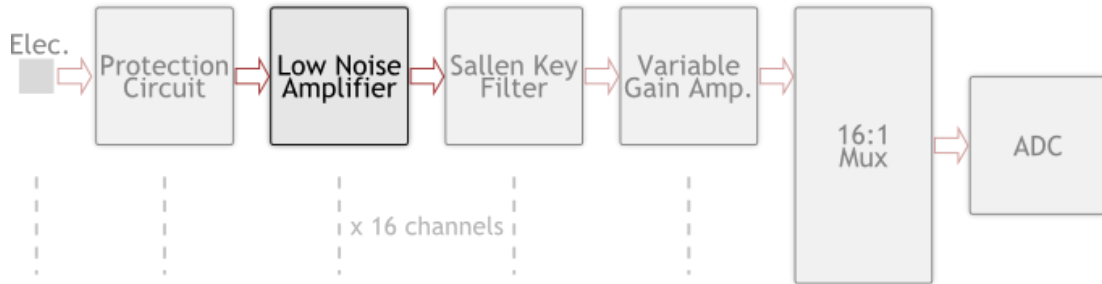


Figure 3.7 The low noise amplifier is the first real stage of filtering and amplification in the system.

Our main concern for this stage is the noise performance. As we demonstrated in the previous chapter, the configuration that has the lowest input referred noise is the passive high pass filter input, which shows a very low $1 \mu\text{V}_{\text{RMS}}$ input referred noise. Our custom architecture is strongly inspired by this configuration.

Figure 3.8 shows the circuit schematic of the AFE unit. The input stage is a passive high pass filter realized by C_1 and R_4 which has a 3 dB high pass corner frequency of

$$f_{-3dB} = \frac{1}{2\pi R_4 C_1} = \frac{1}{2\pi \cdot 11.5 \cdot 10^6 \cdot 6 \cdot 10^{-6}} \cong 2.3 \text{ Hz}. \quad (3.5)$$

The next stage is a low pass filter realized using a non-inverting operational amplifier configuration with the gain dependent on R_6 and R_7 and the low pass corner frequency dependent on both the operational amplifier internal gain bandwidth product and the feedback capacitor C_2 . The gain provided is 46 dB between 2.3 Hz and 36 kHz.

The input resistance has no effect on the overall frequency response and protects the clamping diodes of the operational amplifier during voltage pulses. Figure 3.9 shows the frequency response of the LNA including the input high pass filter.

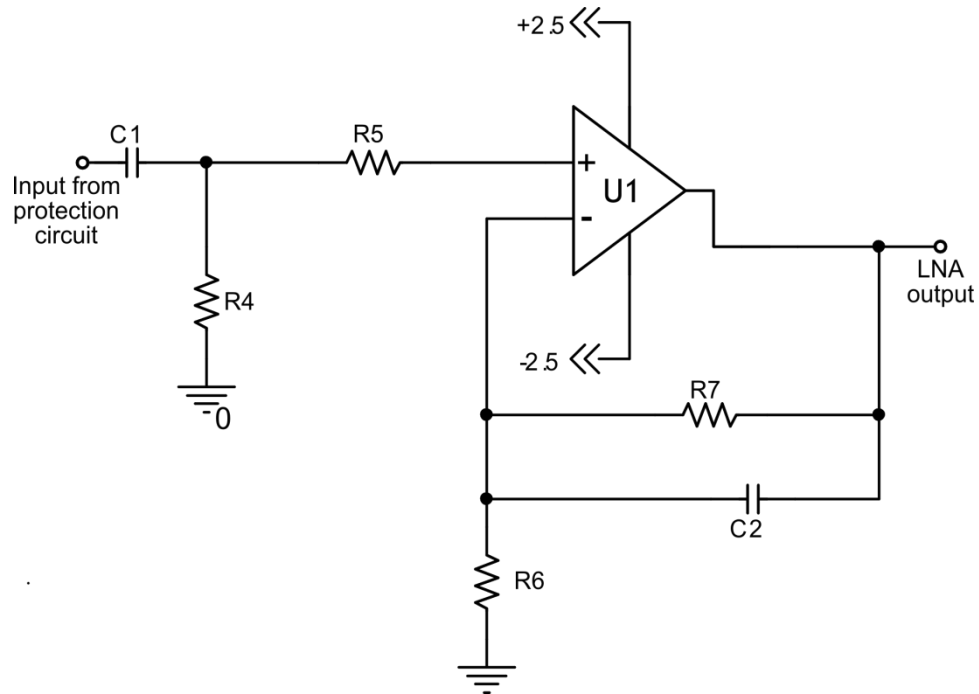


Figure 3.8 The LNA circuit schematic with the high pass input filter realized by $C_1=6\text{ nF}$ and $R_4=11.5\text{ M}\Omega$, the protection resistance $R_5=100\ \Omega$ and the active low pass filter made of U_1 (AD8655, Analog Devices), $R_6=270\ \Omega$, $R_7=53.6\text{ k}\Omega$, and $C_2=62\text{ pF}$.

We can use a simulator like PSpiceTM to evaluate the stability of the circuit. Based on the method from Rosenstark in [51] the estimated phase margin is 92° which guarantees the stability of the system. Figure 3.10 shows the output noise density when considering both the protection circuit and the LNA. PSpiceTM models of the components that were used are included in Appendix I. The plot shows how most of the noise contribution arises from the Flicker noise typical of the operational amplifier. The calculated input referred noise is

$$N_{in,RMS} = \sqrt{\int (Output\ noise\ density)^2 / Gain} \quad (3.6)$$

which is $1.42 \mu V_{RMS}$ over the 1 Hz to 100 kHz band for a gain of 46 dB (i.e. about 199 V/V). This is a worst case scenario compared to our real bandwidth of 2.3 Hz to 36 kHz which will result in less noise in the system.

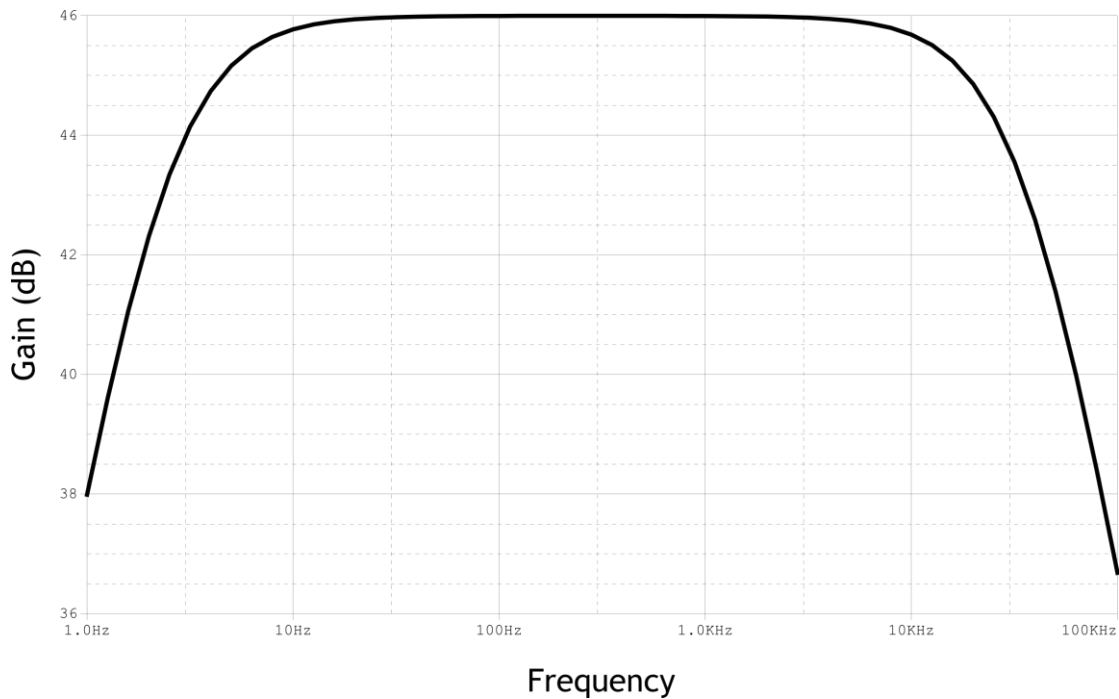


Figure 3.9 Simulated frequency response of the low noise amplifier. Simulation performed using PSpice™.

3.3.3 The Sallen & Key Filter

The first stage of filtering and amplification described above presents features of a first order low pass filter. While this seems to be enough filtering for the noise performance of the circuit, it is preferable to add a second order low pass filter after the preamplification stage (Figure 3.11) in order to reduce the aliasing during the sampling of

the signal by the ADC. The configuration that we considered is a called a Sallen & Key filter as suggested in [23].

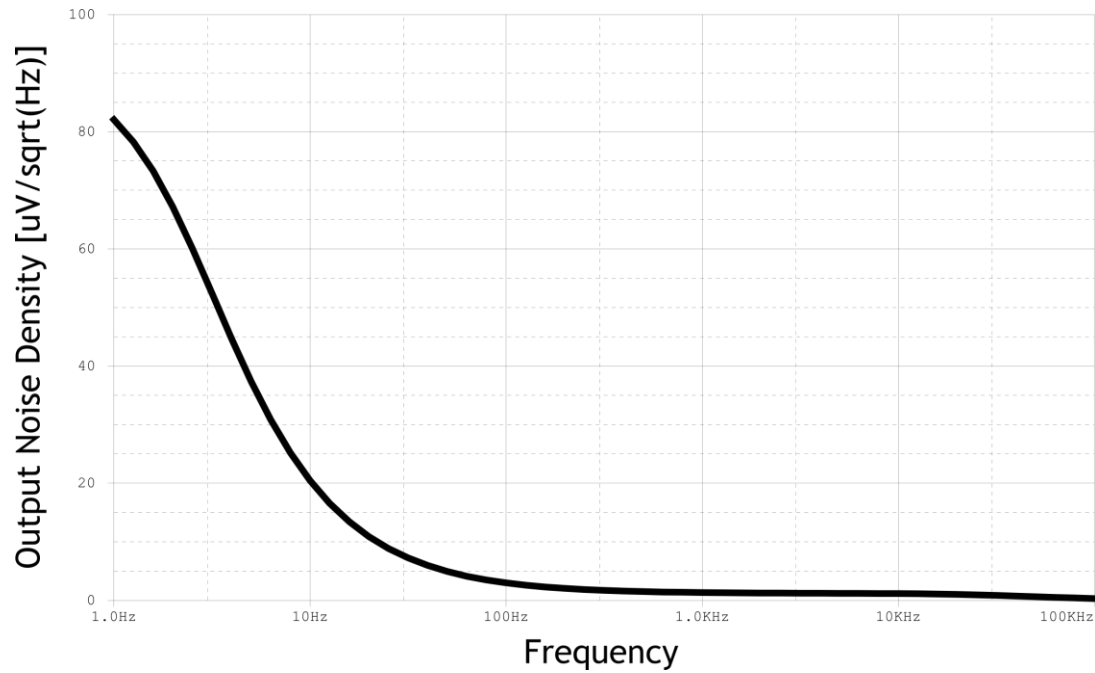


Figure 3.10 Simulated output noise density considering the protection circuit and the LNA. Simulation performed using PSpice™.

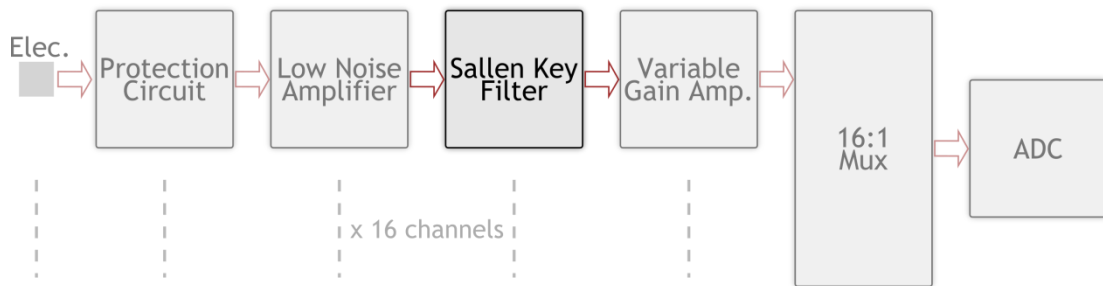


Figure 3.11 The Sallen & Key filter after the preamplification stage to reduce aliasing in by the ADC downstream.

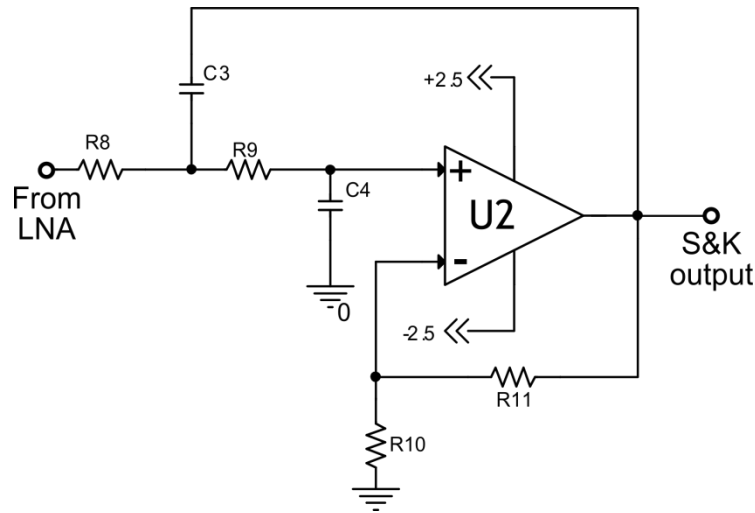


Figure 3.12 Circuit schematic of the second order Sallen & Key filter. R_8 and R_9 are $680\ \Omega$, R_{11} is $124\ \Omega$, R_{10} is $210\ \Omega$, C_2 and C_4 are $18\ \text{nF}$, U_2 is the operational amplifier TSV992 (ST Microelectronics, Geneva, CH).

The filter features a corner frequency of $12\ \text{kHz}$, a gain of $1.60\ \text{V/V}$ (i.e., about $4\ \text{dB}$) and a phase margin of 77° which guarantees stability. The gain value, added to the LNA gain of $46\ \text{dB}$, provides a total gain of $50\ \text{dB}$ for the first two stages of the AFE.

3.3.4 The Variable Gain Amplifier

The output of the second order filter then feeds a variable gain amplifier (Figure 3.13) that is software programmable and provides an additional gain of between $11\ \text{dB}$ and $50\ \text{dB}$.

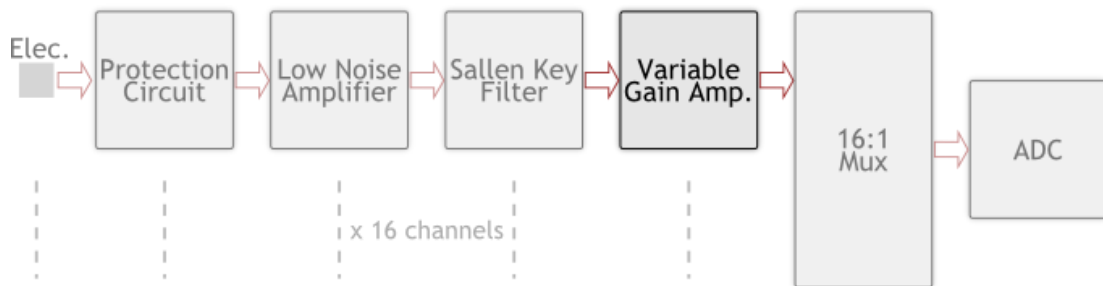


Figure 3.13 The variable gain amplifier in the amplification chain.

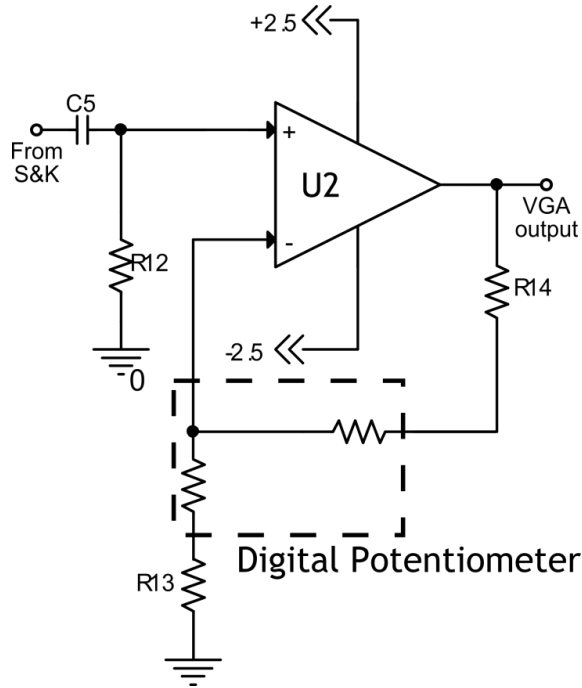


Figure 3.14 Circuit schematic of the variable gain amplifier. C_5 is 6 nF, R_{12} is 1.5 M Ω , R_{13} is 120 Ω , R_{14} is 27 K Ω , the digital potentiometer AD5200 (Analog Devices) has a full scale nominal value of 10 k Ω , U_2 is an operational amplifier TSV992 (ST Microelectronics).

The VGA is ac coupled to the previous stage in order to deal with the operational amplifier's offset voltage. The LNA and the Sallen & Key filter can present tens of millivolts of offset that would saturate the VGA output. The input high pass filter has a corner frequency of about 18 Hz. The VGA architecture is a standard non-inverting configuration that provides the following minimum and maximum gain levels:

$$G_{min} = 1 + \frac{R_{14}}{R_{13} + R_{DP,nom}} = 1 + \frac{27k\Omega}{120\Omega + 10k\Omega} = 3.7 \quad (3.7)$$

and

$$G_{max} = 1 + \frac{R_{14} + R_{DP,nom}}{R_{13}} = 1 + \frac{27k\Omega + 10k\Omega}{120\Omega} = 309 \quad (3.8)$$

where $R_{DP,nom}$ is the nominal full-scale value of the digital potentiometer. The minimum value of 3.7 V/V corresponds to about 11 dB, while the maximum value of 309 corresponds to about 50 dB. The maximum gain for the whole chain is

$$G_{tot,dB} = G_{LNA,dB} + G_{S\&K,dB} + G_{VGA,dB} = 46 + 4 + 50 = 100 \text{ dB} \quad (3.9)$$

while the minimum gain is 61 dB. The minimum gain for the VGA output of 11 dB has been imposed on the design due to the fact that the operational amplifier used is not unit gain stable [52] and a minimum required gain of 3 V/V must be considered.

The digital potentiometer features a standard serial *SPI* interface that enables programming from the FPGA. The *SPI* clock is only provided during the gain programming stage before the measurement because we have measured a cross talk between the clock line and the VGA output that reduces the recorded signal quality. Figure 3.15 shows the frequency response of the whole protection, amplification and filtering stages, from the electrode to the VGA output. The analog condition circuits provide a maximum gain of 100 dB over a 18 Hz to 12 kHz bandwidth.

The simulated output noise for the circuit is 76 mV_{RMS} between 1 Hz and 100 kHz which corresponds to an input referred noise of 0.76 μV_{RMS} before 100 dB (i.e. 100000 V/V) of amplification.

$$Noise_{eq,input} = \frac{Noise_{output}}{Gain} = 0.76 \mu V_{RMS} \quad (3.10)$$

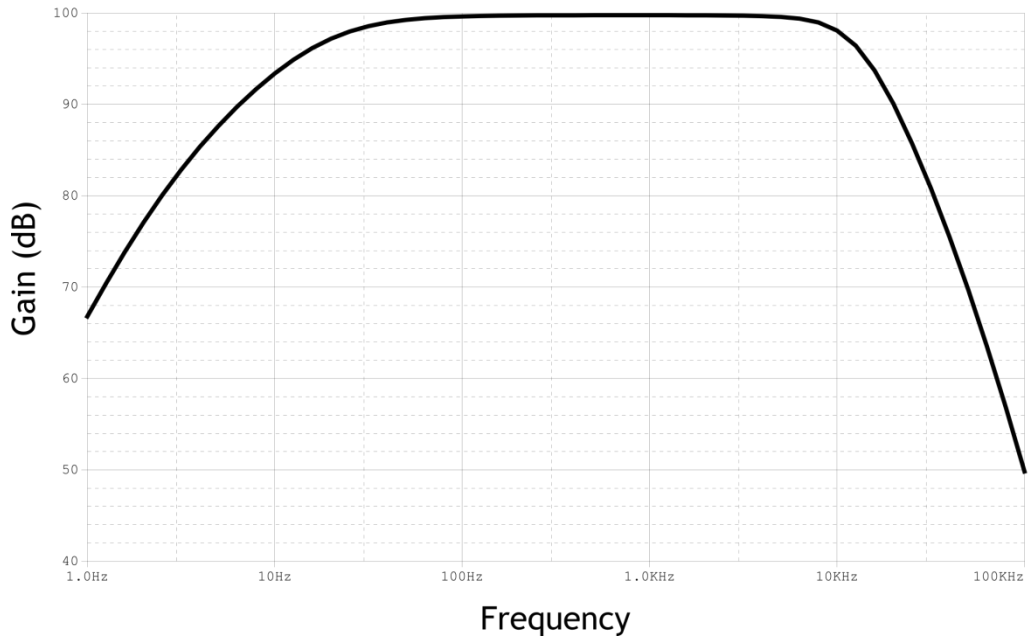


Figure 3.15 Simulated frequency response of the whole analog conditioning chain. This plot takes into account the signal from the electrode to the VGA output. Simulation performed using PSpice™.

3.3.5 The Multiplexing and Data Conversion Unit

After the final stage of amplification the signal is time domain multiplexed and sampled with an ADC so that it can be sent to the FPGA board (Figure 3.16).

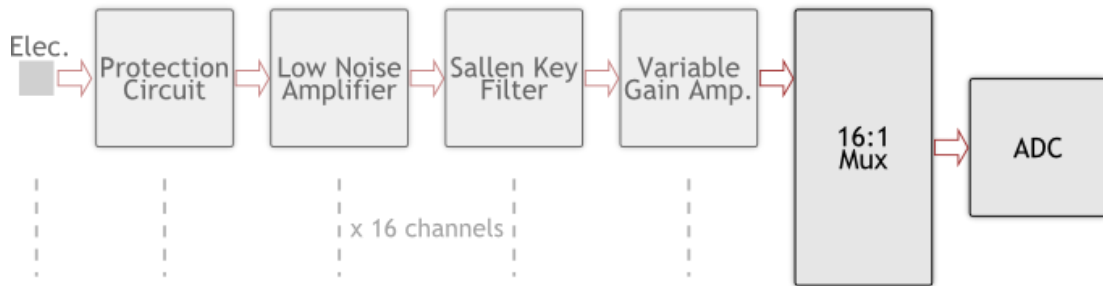


Figure 3.16 The analog multiplexer ends the amplification chain. The output of the multiplexer goes to an analog to digital converter (ADC).

The analog multiplexer ADG706 (Analog Devices) features a 16 channel selectable architecture with a parallel 4 bit interface synchronized with the ADC

recording module. Figure 3.17 shows the circuit schematic for the multiplexing and digital conversion units. The signal from the VGA is bipolar between ± 2.5 V. At the multiplexer output the voltage divider shifts and attenuates the signal, thus the resulting waveform is the exact unipolar replica of the input.

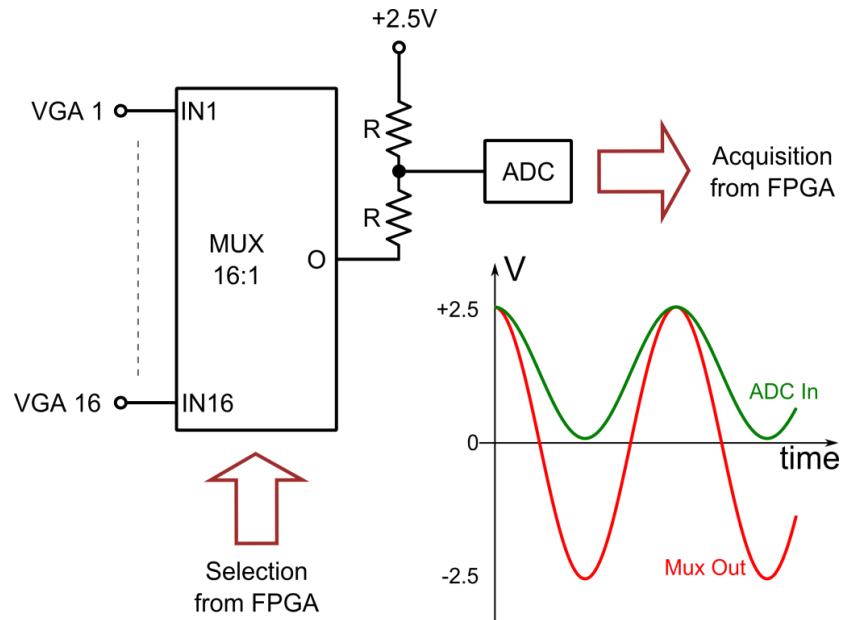


Figure 3.17 Circuit schematic for the TDM and ADC units. The multiplexer is an ADG706 (Analog Devices), ADC is an AD7276 (Analog Devices). Typical waveforms are also shown for reference.

The 16 time domain multiplexed channels are read from the ADC and sampled with 12 bit precision at a rate of 1 Msps, which corresponds to 62.5 kbps per channel. The sampling frequency of more than 5 times the signal frequency assures a low level of signal aliasing.

3.3.6 The Stimulation Circuit

Stimulation voltage has to provide ± 50 V biphasic stimulation pulses (Figure 3.1). The stimulation pulse need not be connected to the recording unit reference voltage, i.e. $STIM^+$ and $STIM^-$ are floating with respect to the recording unit reference voltage. Figure

3.18 shows the circuit diagram of the stimulus generator. The function is controlled by the FPGA through 5 signals: 2 signals that shape the pulse wave form, 3 signals that set the digital potentiometer level and consequently determine the final pulse amplitude.

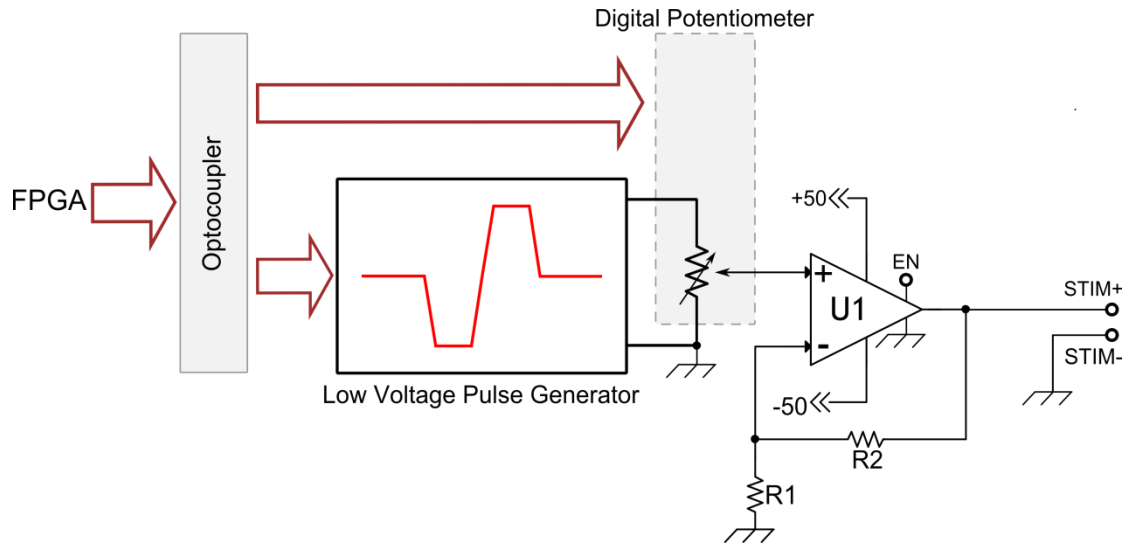


Figure 3.18 A schematic diagram of the stimulation circuit. The digital potentiometer is an AD5200 (Analog Devices) with a nominal value of 10 k Ω , the operational amplifier U_1 is an OPA454 (Texas Instruments), R_1 and R_2 are 1 k Ω and 20 k Ω , respectively. The circuit was designed to provide ± 50 V biphasic output pulses.

Due to the fact that the FPGA is connected to the recording unit reference voltage, i.e. the fluid voltage, the traces go through a stack of octocouplers 6N137 (Fairchild Semiconductors) that isolate the ground planes. The low voltage pulse generator outputs a fixed amplitude low voltage pulse. The rising and falling edge durations of the pulse in Figure 3.1 cannot be varied and is set to 10 μ s. The intervals t_1-t_2 and t_3-t_4 and the time t_5 can be set by the FPGA. The output of the low voltage pulse generator passes through a digital potentiometer connected as a voltage divider. The final stage is a non-inverting configuration with a fixed value of 21 V/V. The output pulse amplitude is configurable by changing the digital potentiometer value between 255 positions. The AD5200 used provides a *SPI* serial interface to the FPGA that can be used to set the desired resistor

value. The maximum pulse amplitude is ± 50 V, the minimum is ± 0.2 V, the resolution of the gain selection of 0.2 V.

The reason why we decided to add the intermediate digital potentiometer instead of placing it on the final stage is that we did not find any device capable of working at ± 50 V while assuring a 255 position *SPI* interface.

The output amplifier features an *EN* pin that can be used to switch off the device, i.e. the output of the amplifier is set to a high impedance. This feature is very useful, because we noted that the output noise of the stimulation circuit itself, connected to the recording unit via a return path through the fluid, caused the recording system to saturate for the highest gain value.

3.3.7 Putting it All Together

The stimulation circuit and the recording channel inputs are interconnected by means of an array of high voltage analog switches (MAX4800A, Maxim Integrated) controlled by the FPGA via a *SPI* interface. Figure 3.19 shows the connection strategy adopted for the single 16 channel module. Two signals come from the stimulation board to the recording unit which also acts as the electrode interface: $STIM^+$ and $STIM^-$, which are the positive and the negative stimulation signals, respectively.

$STIM^+$ is connected to the switch bank SW^+ while $STIM^-$ is connected to SW^- . Each switch can be individually opened or closed, via an *SPI* interface from the FPGA enabling a very flexible stimulation pattern, where the pulse can be sent to any single electrode of each bank of 8, or a group of electrodes can be selected together and closed at the same time to enlarge the stimulation area (thus reducing selectivity) or to reduce the current through the single path when higher voltage pulses are applied.

This configuration also enables the possibility of fast switching between two different stimulation electrodes. The programming time of the switching array can be as low as 5 μ s and the transition time between the closed state of two different switches after programming is on the same order.

This means that once we have sent a pulse to an electrode, e.g. El_1 , we can send another pulse to a different electrode, e.g. El_5 , after only tens of microseconds. Considering the pulse duration of hundreds of microseconds and the AP duration, which is typically about 1 ms in most cases, this a perfectly acceptable time for tests in the field of neural path regenerations [1].

3.4 The FPGA Based Control Unit

The FPGA control unit is in charge of the following: controlling the whole system timing in such a way that everything, from the stimulation pulse firing timing to the start of recording, is well coordinated and synchronized, acquiring data from the custom electronic board that features *on-board* ADC, sending data to a PC for persistent storage and successive post processing and data analysis, setting all the experiment parameters, like the recording channel gain, the stimulation pulse amplitude, the number of pulses to fire, etc.

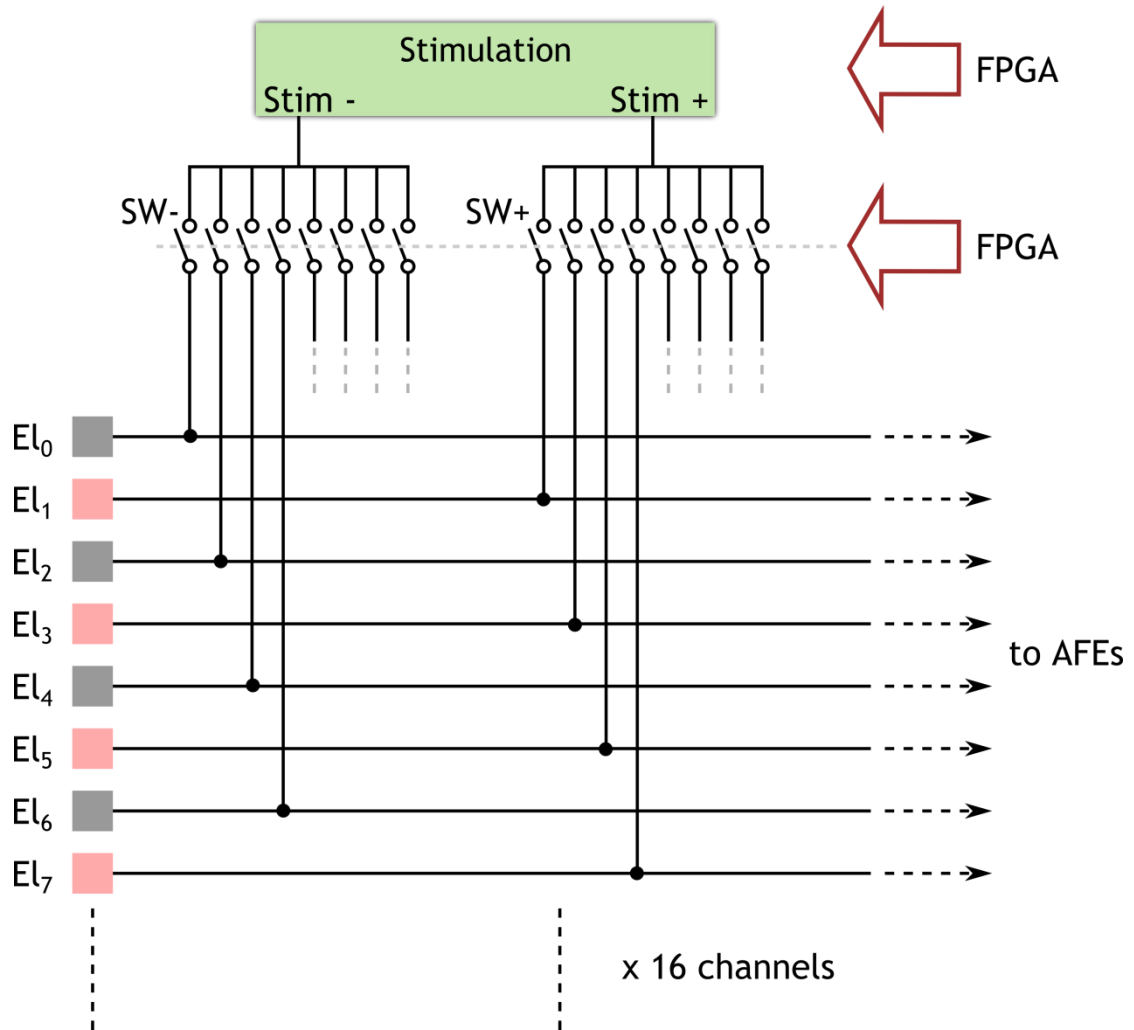


Figure 3.19 The switching matrix for connection of the stimulation circuit to the electrodes. SW^+ and SW^- are MAX4800A (Maxim Integrated) fast switches.

Figure 3.20 shows a block representation of the complete FPGA control unit designed and programmed to manage the full system. Instead of realizing our own FPGA board, we acquired a commercially available piece of hardware (Atlys Development Board, Digilent Technologies) which is well suitable for academic and research utilization and features a very impressive number of functionalities.

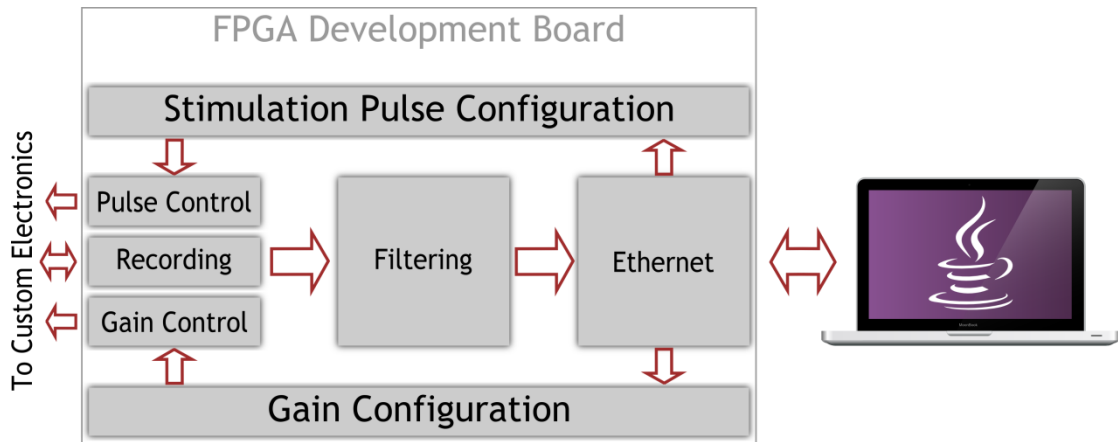


Figure 3.20 A high level architecture overview of the FPGA control unit.

In the next section we describe the FPGA development board used to highlight the modules that we used in order to accomplish our tasks. In the sections that follow instead we will present the single module unit that composes the firmware. The code for the modules described in this section can be found in Appendix B.

3.4.1 The Atlys FPGA Development Board

The Atlys is a development board based on a *Field Programmable Gate Array (FPGA)* that features a Xilinx Spartan-6 LX45 FPGA on-board. Figure 3.21 shows a top view of the board and the main available modules that we used are highlighted.

While this board presents many I/O modules for several uses, from HDMI signal transferring to USB communication controllers, we used a reduced subset of these features to accomplish our task.

The communication between the control board and the custom designed electronic system consists of a 68 pin VHDCI connector that routes to the external system up to 40 FPGA I/O pins. The I/O are configured to operate as *Low Voltage CMOS signals (LVCMOS25)* at 2.5 V, the outputs are protected using resistors from over voltages. The connector routes both the signals that control the system functioning and the *SPI* data

from the recording modules that contain the acquired action potentials. The maximum clock frequency on these lines is 16 MHz.

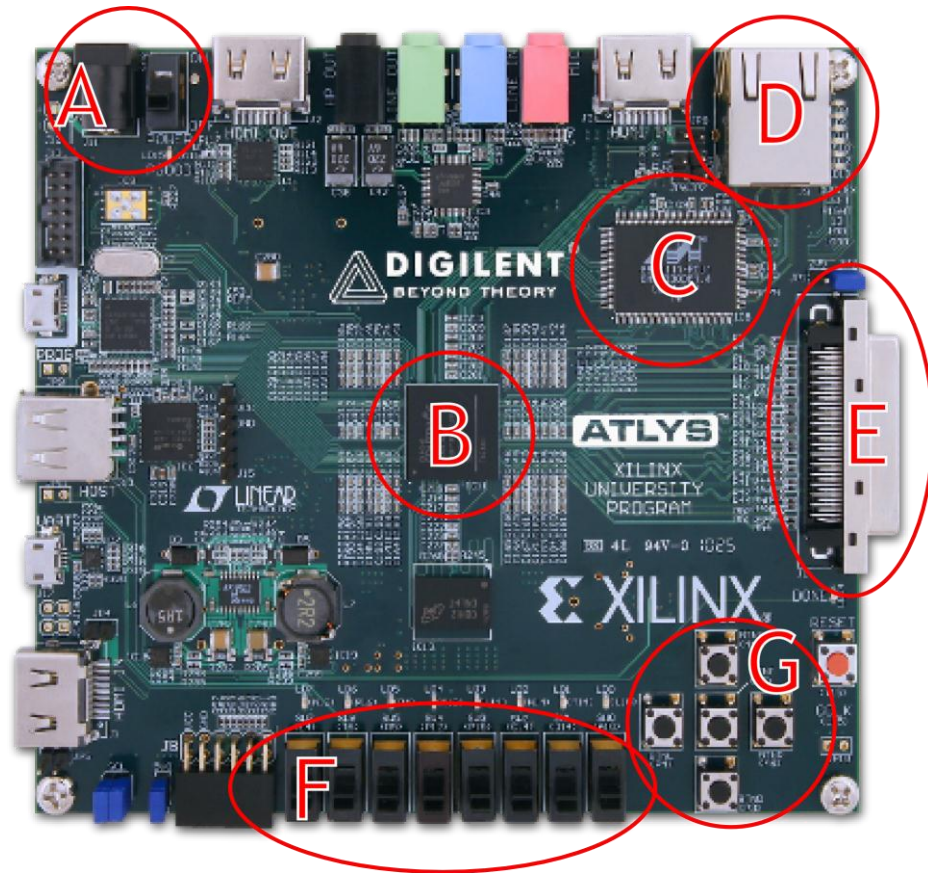


Figure 3.21 The Digilent Atlys FPGA development board. A, the power supply connector; B, the FPGA Xilinx LX45; C, the chip for Ethernet interfacing the Alaska 88E1111 (Marvell); D, the Ethernet RJ-45 connector; E, the VHDCI connector for interfacing with the custom electronics; F, 8 switches connected to FPGA's input and G, on-board programmable buttons connected to FPGA ports used for system test.

In order to realize Ethernet communication, the board relies on a chip from Marvell that is in charge of managing the interface physical layer. It is a transceiver that can work at the three standard Ethernet speeds: 10, 100 and 1000 Mbps in both *Half Duplex* and *Full Duplex* mode; moreover, it is capable of auto-negotiation with the others devices of the Ethernet network that is connected to decide the best suitable configuration, speed and mode to use. It is compliant with IEEE 802.3 Ethernet

specifications and expands these functionalities with Marvell proprietary features that we did not use for our project.

During the system electrical and biological testing we made extensive use of a bank of 8 switches and 5 buttons that are connected to 13 general purpose I/O pins of the FPGA. The system features an *on-board* CLK system for a maximum FPGA clock speed of 100 MHz in standard conditions. For firmware development and FPGA programming the Xilinx ISE Design Suite SDK was used and is available from the manufacturer website.

3.4.2 The Gain Control Unit

The system gain control unit uses a 3 bit standard *SPI* interface to program the gain of all of the 64 channels at once. All of the channels are programmed to the same gain, it is not possible to have different gains for different channels.

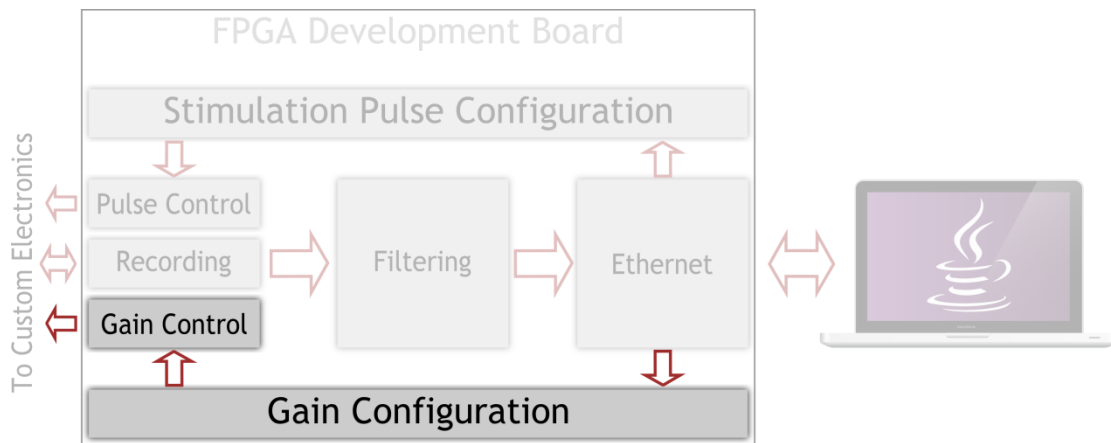


Figure 3.22 The amplification core management unit in the FPGA hierarchy.

The 3 bit interface sets the *on-board* digital potentiometers discussed above to one of 255 possible levels that program the channel gain between 61 and 100 dB. The signals

VGA_CS, *VGA_CLK* and *VGA_SDATA* are connected to the respective pin of the 64 variable gain amplifier units, one for each channel.

Data_VGA is the value that is sent through the *SPI* interface to the devices and can be read either from the *on-board* switch bank during testing or from the Ethernet interface in order to enable gain programming from the pc.

Prog_VGA initiates the actual programming of the device. *VGA_CLK* is active only during the actual time of programming and is held to logic 0 otherwise.



Figure 3.23 Block diagram of the amplifying gain control unit.

The programming sequence is driven by a 390 kHz clock line generated by the FPGA core from the main 100 MHz clock for a total programming time of less than 200 μ s. Gain programming is typically set once before the measurements are conducted and then left fixed.

3.4.3 The ADC Data Acquisition Unit

The ADC reading unit is one of the core modules of the system and is in charge of acquiring converted data from the four 16 channel electronic modules. Figure 3.24 shows a block diagram representation of the ADC data acquisition module within the whole system.

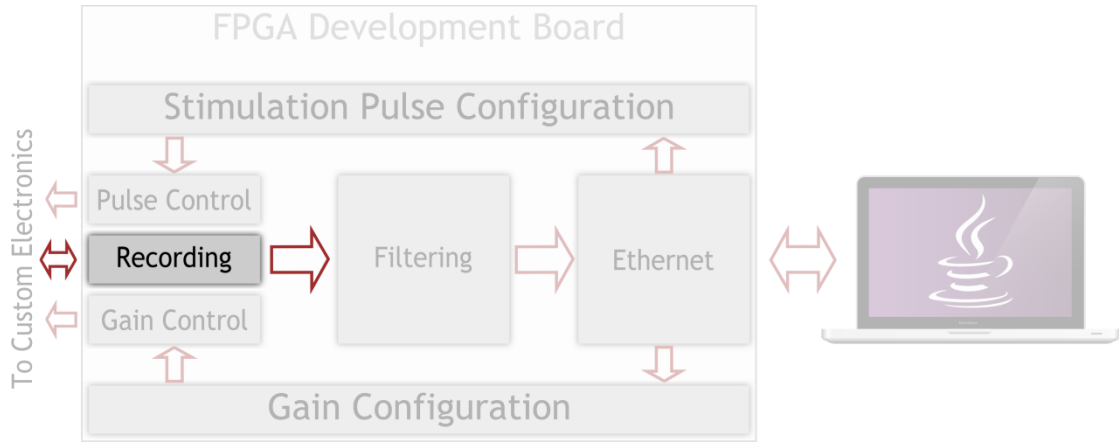


Figure 3.24 Block diagram of the ADC unit directly connected to the custom electronics.

Figure 3.25 shows the input and output scheme of the module. The ADC module is driven by a 16 MHz *Clk* signal which sets the timing of the conversion and the sampling frequency. When the signal *Start* is set high, the module resets itself and starts the acquisition process sending *SPI_CLK* (16 MHz) and *SPI_CS* to the 4 ADCs on the four (4) 16 channel modules. These signals are unique for the four boards. The ADC requires 16 *SPI_CLK* clock cycles to complete its 12 bit measurement of the input. At each clock cycle data enters the module via the four SPI serial inputs *SData1...SData4*, one for each module. *A0,A1,A2* and *A3* are used to drive the multiplexer that selects the channel to the ADC: *A0-A1-A2-A3 = 0000* means that channel 1 is connected to the ADC input, *A0-A1-A2-A3 = 0001* means that channel 2 is connected to the ADC input and so on for the 16 channels. When the 16th channel is sampled the counter starts again from 0000 feeding the ADC with the first channel once again. The number of clock cycles required to sample one single channel is 16, which for a 16 MHz master clock gives a sampling rate of

$$F_s = \frac{16MHz}{16 \text{ cycles} \cdot 16 \text{ channels}} \cong 62.5 \text{ ksps}. \quad (3.11)$$

As the serial stream of data comes the *most significant bit (MSB)*, first from the four *SData* lines connected to the ADC, the module converts the serial stream to parallel and, when all the 16 bit have arrived, it outputs the parallel records on the 16 bit busses *Q1-Q4* and sets *Load* high to acknowledge to the other modules down the line that a new measurement on one channel of the four electronic boards are ready to be processed. The ADC works at 12 bit of resolution but the data that it sends back on the *SPI* line is 16 bit, zero padded with two zeros at the beginning and two zeros at the end.

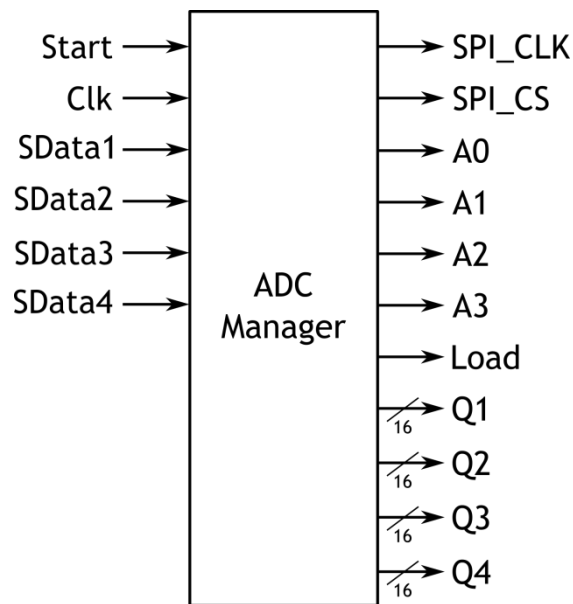


Figure 3.25 The input and output scheme of the ADC manager.

3.4.4 The Digital Filtering Unit

Figure 3.26 and Figure 3.27 show filtering in the processing chain and the I/O port schematic, respectively.

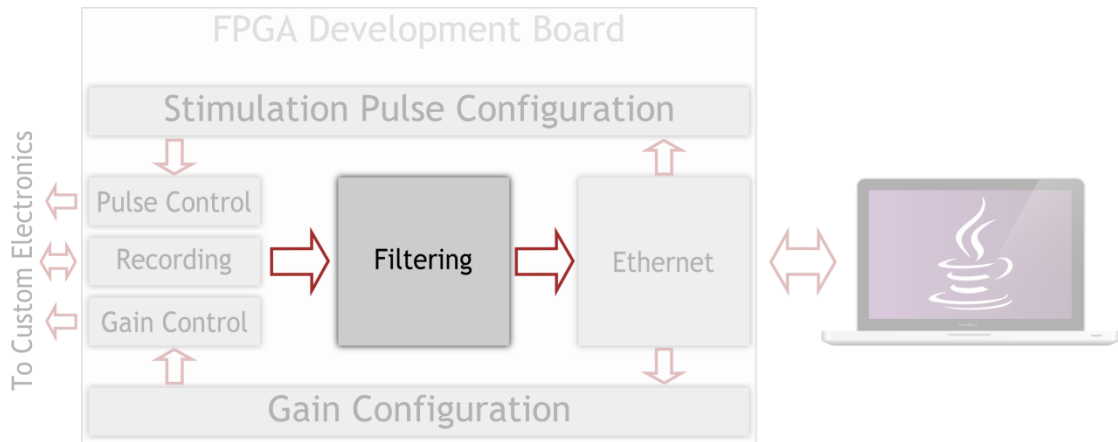


Figure 3.26 Block diagram of the system with the filtering stage after the data acquisition module.

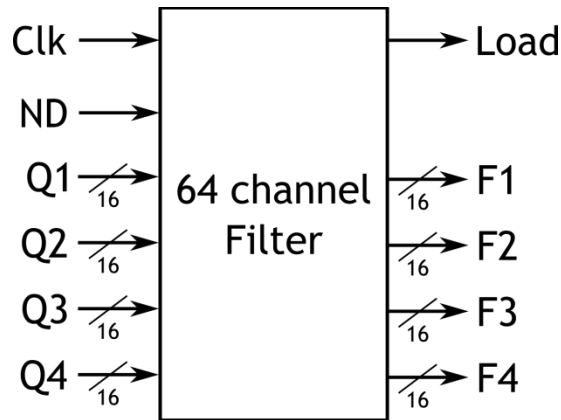


Figure 3.27 The I/O scheme of the filtering module.

The four 16 bit busses from the ADC acquisition modules represent the input of the filtering stage; each of these 16 bit busses are the time domain multiplexed sequence of recording from the 16 channels sequentially from one single acquisition board. The pin *ND* is connected to the *Load* output of the previous *ADC* management stage and, when it is set high, causes the filter to take in the next sample to read. The *Clk* signal is 100 MHz.

The filter was first designed and simulated in MatlabTM. It is a *Finite Impulse Response (FIR)* realized using a Kaiser window approach [57] to generate a 274 parameters impulse response $h(n)$ (Figure 3.28).

Figure 3.29 shows the frequency response of the filter calculated in Matlab for the impulse response considered. The filter features a 30 Hz to 10 kHz bandwidth for a sampling frequency of 62.5 ksps.

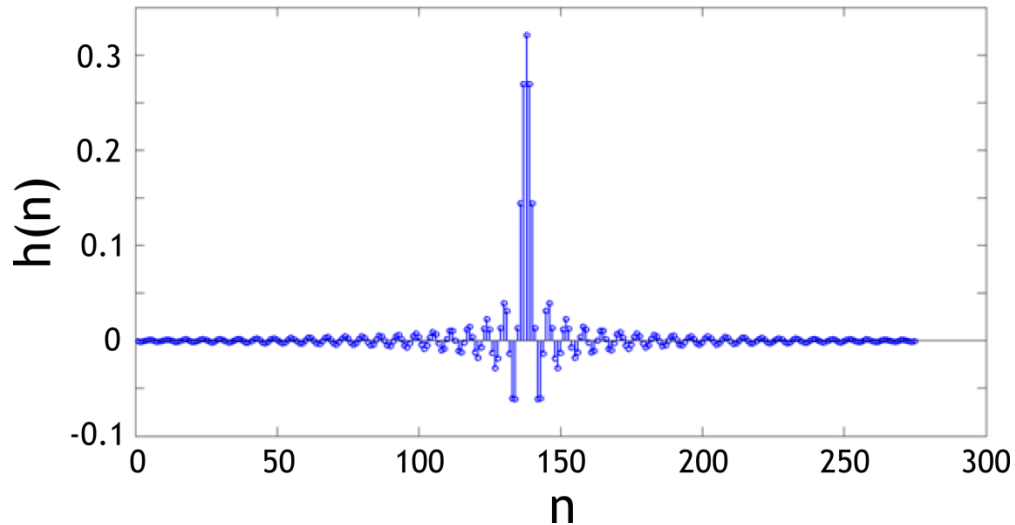


Figure 3.28 The 274 samples of the impulse response using the Kaiser window method. $h(n)$ is the vector of points that forms the impulsive response vs. point n . Simulation performed using Matlab™.

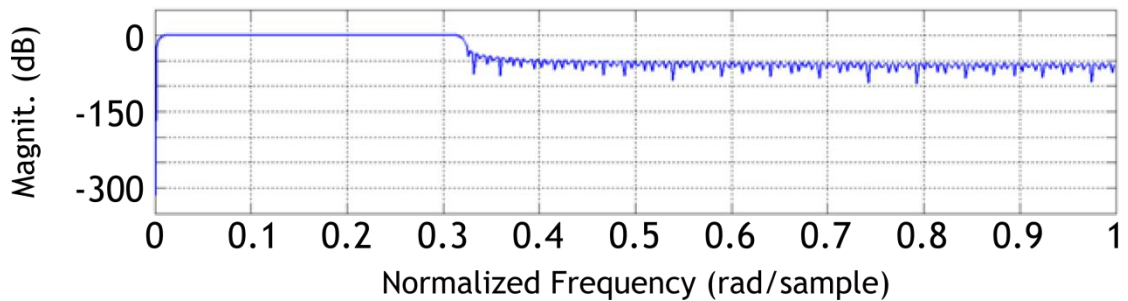


Figure 3.29 The frequency response of the digital FIR filter. Simulation performed using Matlab™.

Once the impulse response array from Matlab™ is obtained we passed it to the ISE Design Suite internal tool called FIR Compiler that can generate a filter with the desired number from the input impulse response. We let the tool generate the module for the time domain multiplexed input stream from the ADC.

The filter has an intrinsic delay that corresponds to the number of samples in the impulse response (in our case 274) multiplied by the time between two consecutive input from the same channel, which in our case corresponds to:

$$Delay = 274 \cdot 1/62.5kHz = 4.3 \text{ ms.} \quad (3.12)$$

Once the filtered samples are ready at the output, the module acknowledges the successive units by setting high the bit *Load*.

3.4.5 The Ethernet Module

Figure 3.30 highlights the Ethernet module after the filtering stage which accomplishes the task of sending all the recorded data to the PC via *UDP* packets. The stream of bytes from the filtering module is packed into chunks of 1440 bytes each, headers are added and the whole packet, featuring a *payload* of 1484 bytes, is sent at once over the Ethernet line.

The Ethernet module features internal buffers to temporarily store data from the filtering module while sending the previous packet. This solution increases the fault tolerance of the system in cases when the network is slow or the receiving PC is busy. The protocol used is *UDP* packets, which means that it is very fast, but no error checking is provided: if a packet is lost there is no way for both the receiver and the transmitter to know about this unfortunately.

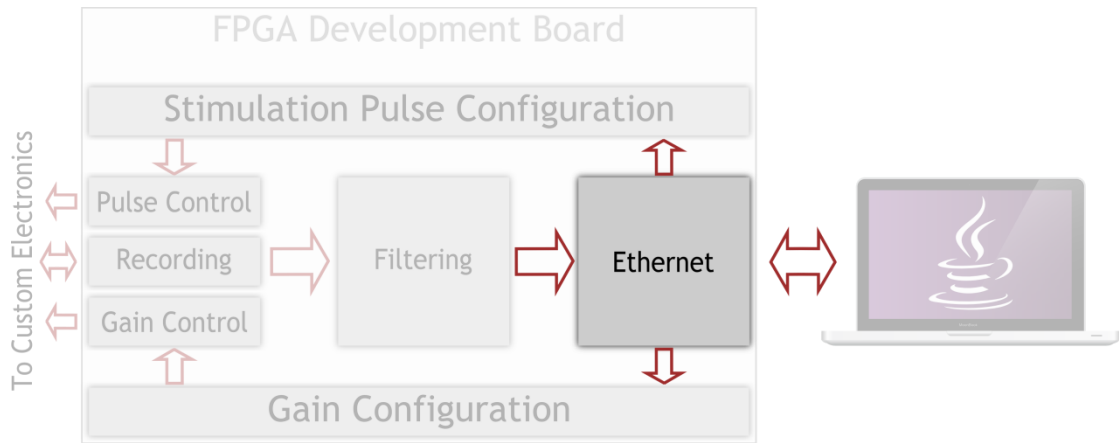


Figure 3.30 Block diagram of the system with the Ethernet module highlighted.

3.4.6 The Java Based Acquisition and Storage Driver

The data sent via *UDP* packets from the Ethernet module are received by a PC running a *Java* based custom driver that receives the payload, extracts the measurements and saves the recordings in a CSV file named after the recording session. The data is now ready to be imported to other tools like Matlab for post processing data analysis.

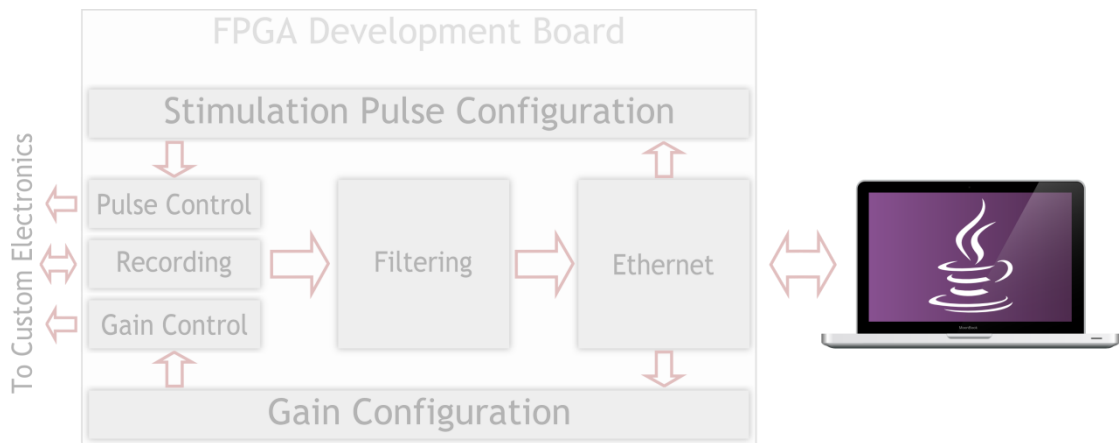


Figure 3.31 The PC receives data from the Ethernet module and transmits the configuration parameters to control the system.

To facilitate the use and configuration of the system a *graphical user interface (GUI)* has been designed and realized which features bidirectional communication between the PC and the FPGA control board. This software relies on a FPGA internal firmware module that receives commands from the PC and manages the different tasks, like gain programming, acquisition initialization or stimulation pulse generation.

Currently the PC software cannot process the recorded data, that is to say that there is not a graphical tool to visualize or analyze data from the system. In order to accomplish this task an external software platform is required, such as Matlab™.

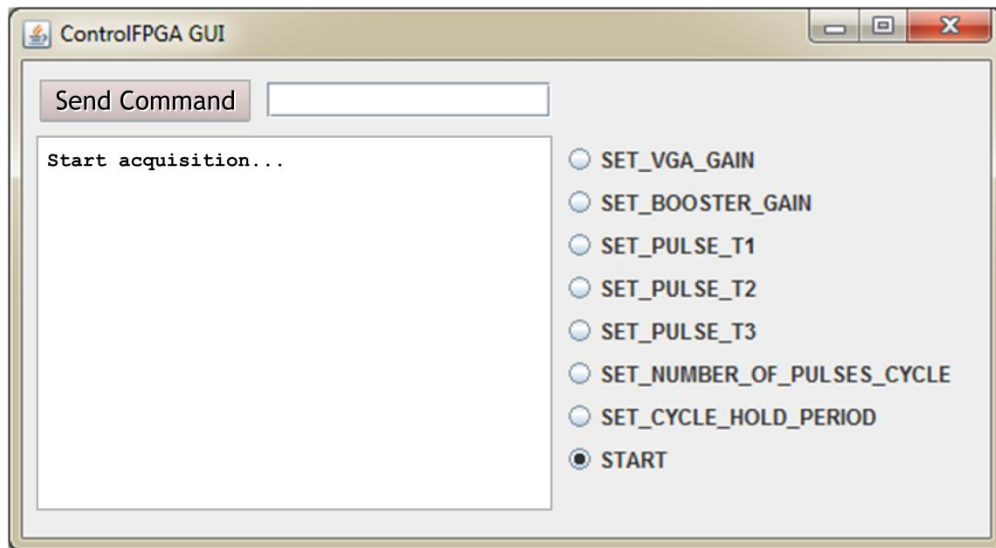


Figure 3.32 The *GUI* for system configuration and acquisition initialization.

3.5 Summary

In this chapter the design, simulation and realization of the different units was presented that, when assembled together, forms the whole bi-directional electronics system. The system designed features 64 channels spread over four identical 16 channel modules. Each channel is connected to a single electrode and includes a protection circuit to increase the impedance of the system even during stimulation pulses, a low noise

amplifier, a Sallen & Key second order filter, and a VGA software programmable to 255 different gain level.

The system has been simulated using PSpice™ with the actual electrical model supplied by the component manufacturers and it shows a variable gain between 61 and 100 dB in the 18 Hz to 12 kHz band.

The input referred noise has been analyzed and the result from simulations is extremely low below $1 \mu\text{V}_{\text{RMS}}$. This value doesn't take into account the environmental noise of course, but we will see in the next chapter that the actual measured input referred noise is very similar to this value.

Later in the chapter the whole FPGA control and acquisition software was described with a particular focus on the ADC acquisition and filtering stages. Lastly the PC software has been described that reads data from the Ethernet connection sent via *UDP* packets and saves them to a CSV file. The PC software features bidirectional communication with the FPGA in order to configure the experiment parameters, i.e. gain, pulse amplitude, pulse timing and to start remotely the data acquisition.

CHAPTER 4: ELECTRICAL AND BIOLOGICAL TEST OF THE BI-DIRECTIONAL BMI ELECTRONICS SYSTEM

In order to validate the architecture we realized a board featuring only 3 channels: one for stimulation and two for recording. In this chapter the tests and measurements performed on the system will be reported alongside with the calculation of some important electrical characteristics such as noise, gain and bandwidth.

This chapter first describes the experimental setup we used to characterize the system from an electrical point of view, i.e. the gain and bandwidth of the different stages of the system. The gain across different channels is strongly dependent on the actual value of the components, so an analysis of the gain error that we expect will also be presented and discussed, taking into account the passive component tolerances. Then measurements and calculations of the input referred noise of the system are performed and the Matlab script used to extract the input referred noise from the output noise level will be explained and commented on.

In the second part of the chapter the biological test of the system will be described and evidence of neural activity stimulation capabilities and action potential acquisition will be demonstrated. Moreover this section will report also about a comparison test that we made with a very common commercially available MEA data acquisition tool, the OmniPlex™ from Plexon, and our system. We are pleased to report that the signal fidelity of our system was superior to the commercial system at an order of magnitude less cost (\$70k vs. our estimated cost, for 64 channels, of about \$10k).

4.1 Electrical Test and Characterization

In order to measure the gain and bandwidth of the system we used a digital oscilloscope (Tektronix TDS 1002B) using 2 channels set to 60 MHz, 1 Gs/s, 2.5 k points and a waveform generator (Tektronix AFG3021) set to 1 channel at 25 MHz maximum frequency, 20 mV_{PP} minimum amplitude for a sine wave into a high impedance load. During the electrical characterization of the recording channels the stimulation unit was switched off and disconnected from the system.

During these tests the system was powered with a supply of ±12 V instead of ±50 V because of the lack of commercially available voltage regulators that can work at that voltage.

4.1.1 Gain Considerations and Measurements

The gain of a single channel depends, as expected, on the tolerance of the values of the single channel's components. In particular the passive resistors that determine the gain of the three non-inverting stages that compose the whole amplification chain. Figure 3.8, Figure 3.12 and Figure 3.14 show the circuit diagram of the *LNA*, the Sallen & Key filter and the *VGA*, respectively. For the first two stages the gain value is given by

$$Gain_{LNA} = 1 + \frac{R_7}{R_6} \quad (4.1)$$

and

$$Gain_{S\&K} = 1 + \frac{R_{11}}{R_{10}} \quad (4.2)$$

while for the third stage, of the *VGA* we have to consider two different cases when the digital potentiometer is set to the maximum and to the minimum gain:

$$Gain_{VGA,max} = 1 + \frac{R_{14} + R_{DP,nom}}{R_{13}} \quad (4.3)$$

where $R_{DP,nom}$ is the nominal full scale value of the digital potentiometer and

$$Gain_{VGA,min} = 1 + \frac{R_{14}}{R_{13} + R_{DP,nom}} \quad (4.4)$$

Assuming a tolerance of $\pm 1\%$ for R_6, R_7, R_{10}, R_{11} , $\pm 5\%$ for R_{13} and R_{14} , and $\pm 30\%$ for the digital potentiometer full scale value we estimated the nominal, minimum and maximum gain value expected from each amplification stage. The values are listed in Table 4.1. In order to measure the gain at the different stages of amplification chain we had to separate the *LNA* and *Sallen & Key* stage from the *VGA* because the lowest input signal we could generate with the function generator AFG3021 would have been saturated the output of the *VGA* when it was set at the maximum gain. The function generator was used to output a 1 kHz sine wave with 20 mV_{pp} of amplitude, the lowest value possible for this instrument. Using a 10 k Ω potentiometer as a voltage divider we reduced the signal amplitude to a value small enough for the input signal while still being slightly above the noise level. Figure 4.1 shows the input signal generated by the function generator and attenuated by an analog potentiometer and the relative output of the *Sallen & Key* filter that shows how the noise is considerably filtered out.

In the case of the *VGA* gain the two cases were measured for high gain and low gain settings. While measuring this stage, we connected the function generator to the *VGA* input and disconnected the amplification chain before the input node. The output was measured at the operational amplifier pin.

Table 4.1 Calculated and measured gain values for the different amplification stages

<i>Stage</i>	<i>Nom*</i> [V/V]	<i>Min*</i> [V/V]	<i>Max*</i> [V/V]	<i>Nom*</i> [dB]	<i>Min*</i> [dB]	<i>Max*</i> [dB]	<i>Meas*</i> [dB]
<i>LNA</i>	200	196	203	46.00	45.83	46.17	46.10
<i>S&K</i>	1.52	1.51	1.53	3.62	3.56	3.68	4.00
<i>VGA, low</i>	309	260	364	49.80	48.30	51.20	48.83
<i>VGA, high</i>	3.67	2.95	4.99	11.30	9.40	14.00	11.3

* The values are the nominal, the minimum and the maximum calculated values in V/V and decibel and the measured values in decibel. The last column is the measured value during our tests.

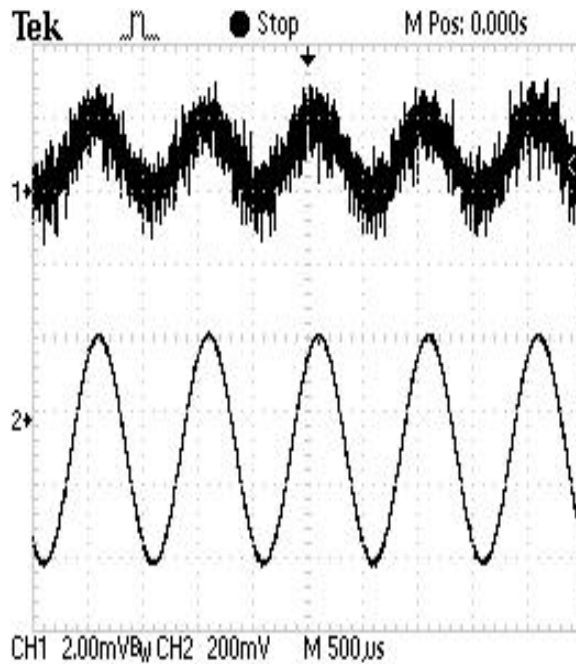


Figure 4.1 The measured test signal before and after the first stage of amplification. CH1: the input of the *LNA* from the function generator, CH2: the output of the *Sallen & Key* filter. Note the measured gain is about 320 V/V.

We can easily calculate the total gain which is 98.93 dB instead of the expected 100 dB value. This is due to the tolerances on the passive component values that can slightly modify the final gain, as expected.

4.1.2 Bandwidth Measurement

In order to measure the bandwidth we followed the same procedure described in the previous section, separating the three stages into two blocks, the first one including the *LNA* and the *Sallen & Key*, and the second one being only the *VGA* amplifier. The measurements were performed for this last stage at the full maximum gain, which corresponds to a nominal value of 50 dB. The value assumed as the reference gain to estimate the -3 dB bandwidth was 1 kHz. It is worth to point out that when converting the gain units from *V/V* to *dB*, being that the values are voltages and not power, we use the relation

$$Gain_{dB} = 20 \cdot \log_{10} \left(\frac{V_{out}}{V_{in}} \right) = 20 \cdot \log_{10}(Gain_{V/V}) \cdot \quad (4.5)$$

From (4.5), if we subtract 3 dB we obtain

$$\begin{aligned} 20 \cdot \log_{10} \left(\frac{V_{out}}{V_{in}} \right) - 3 \text{ dB} \\ &= 20 \cdot \log_{10}(Gain_{V/V}) - 20 \\ &\quad \cdot \log_{10} \left(10^{3/20} \right) \\ &= 20 \cdot \log_{10}(Gain_{V/V}) - 20 \cdot \log_{10}(\sqrt{2}) \\ &= 20 \cdot \log_{10} \left(\frac{Gain_{V/V}}{\sqrt{2}} \right) \end{aligned} \quad (4.6)$$

which means that, because we are considering implicitly *dB_V*, the gain is reduced of a factor 0.707 instead of being reduced to the half (i.e. 0.5).

The actual measurement was performed following the steps below:

1. The function generator was set to output a sine wave with a frequency of 1 kHz that was connected to the input pad of the particular stage under

test;

2. The output of the stage under test was connected to the oscilloscope operating to measure the signal's *Fast Fourier Transform (FFT)*. The output value at 1 kHz was taken as the reference gain in *dB* and is named G_0 ;
3. The frequency of the signal from the function generator was changed toward the lower frequency value until the gain value measured by the oscilloscope cursor was exactly equal to G_0 (i.e., - 3 *dB* point). The corresponding value of the frequency was the high-pass $f_{.3db}$ for the stage under test;
4. Using the same procedure we identified the low-pass frequency moving the generated signal frequency toward higher values.

For the first stage composed of the *LNA* and the *Sallen & Key* filter the corner frequencies measured were 2 Hz for the high pass cut-off frequency and 13 kHz for low pass cut-off. For the *VGA* stage the bandwidth measured was 14 Hz to 80 kHz. The resulting global bandwidth of the system was therefore 14 Hz to 13 kHz, which is slightly broader than the expected 18 Hz to 12 kHz. This difference can be due to the tolerance of passive component values and to the fact that the model that we used during the simulations we performed may not be completely correct. For example, the operational amplifier internal poles and the characteristic intrinsic *gain bandwidth product (GBP)* may be slightly different than the specification values.

4.1.3 Input Referred Noise Measurement

A common way to measure the noise performance of a circuit for this kind of application consists of connecting the input to the ground reference voltage and

measuring the output V_{RMS} value [5], [23] and [44]. The procedure that we followed to measure the input referred noise is reported here.

The input of the electronic system corresponds to the pad connected to the electrode after connecting the input of the *AFE*. The noise signal in Figure 4.2 can be used to extract the output noise figure of the system by simply using Matlab to import the data and calculate the standard deviation, which corresponds to the V_{RMS} value of the signal. The relation used in Matlab to estimate the standard deviation was

$$std = V_{RMS} = \sqrt{\frac{1}{n-1} \sum_{i=1}^n (x_i - \bar{x})^2} \quad (4.7)$$

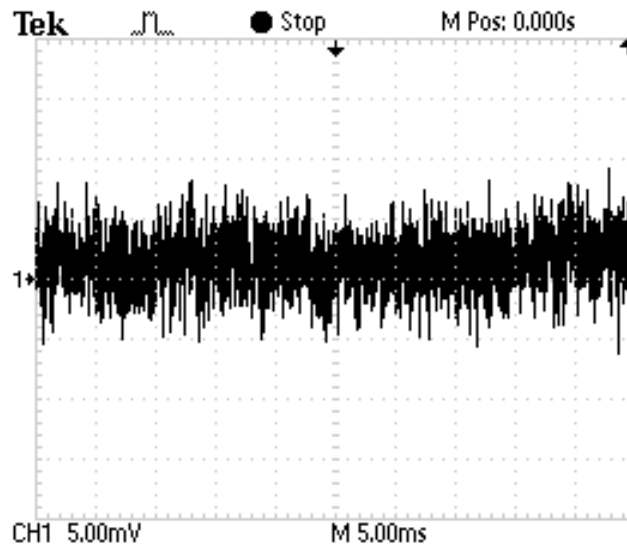


Figure 4.2 A sample of the output noise recorded at the *VGA* output with the input short circuited to the reference voltage. The 5 ms/div horizontal resolution corresponds to a 25 kHz *FFT* bandwidth. Note this data corresponds to a $V_{RMS,input}=1.36 \mu V_{RMS}$.

The value calculated this way is the equivalent *RMS* value of the noise at the output of the amplification chain. If this value is divided by the gain of the channel, we obtain the input referred noise. Table 4.2 shows the measured output noise and the

calculated input noise for two of the measurements performed with different time base resolution. The first one is refers the noise over a 25 kHz bandwidth imposed by the oscilloscope, while the second measurement is for 1.25 MHz.

While the absolute values of the input referred noise are a very good result in that they are below the maximum value allocated from the design specifications, the reader will note that the noise over a larger band (1.25 MHz) is lower than the noise over a band of 25 kHz, while we would have expected the opposite. As a matter of fact an important component of the noise arises from the thermal noise of the components and we would expect it to increase as the bandwidth over which it is measured increases.

Table 4.2 Output and input system noise measured and calculated from time domain recording, respectively.

<i>Horizontal resolution</i>	<i>Bandwidth</i>	<i>Number of samples</i>	<i>Time span</i>	$V_{RMS,output}$	$V_{RMS,input}$
5 ms/div	25 kHz	2500	50 ms	120 mV _{RMS}	1.36 μ V _{RMS}
100 μ s/div	1.25 MHz	2500	1 ms	104 mV _{RMS}	1.18 μ V _{RMS}

**These values are the result of the standard deviation calculation and they do not represent the worst case, discussed below.*

The explanation of this unexpected result can be found by considering the total time interval in which these measurements were recorded, 50 ms for the 25 kHz bandwidth and 1 ms for the 1.25 MHz bandwidth. In fact, as the time per division changes, the number of points acquired remains the same, thus lower frequency variations, i.e. in the order of tens of milliseconds, that may occur can be observed in the first case and may not be seen in the second case. If we divide the first vector into 50 intervals of 1 ms each (so now in both cases we cover the same time span, even if we have a different amount of points) and we recalculate the input noise we have the result in

Figure 4.3. As we can see, at each interval the results can be very different, with a worst case for the input referred noise being $1.6 \mu\text{V}_{\text{RMS}}$. While this result is perfectly in line with the specifications, it is evident that it is notably larger than the value expected from simulations, which was $0.76 \mu\text{V}_{\text{RMS}}$. This deviation can be interpreted in two ways, both of which are quite realistic. The noise simulations are based on the PSpiceTM component models released by the manufacturers, which does not fit completely the actual device performance. Furthermore, the simulations do not take into account the environmental noise and all of the other noise sources, like the power supplies and the FPGA interface.

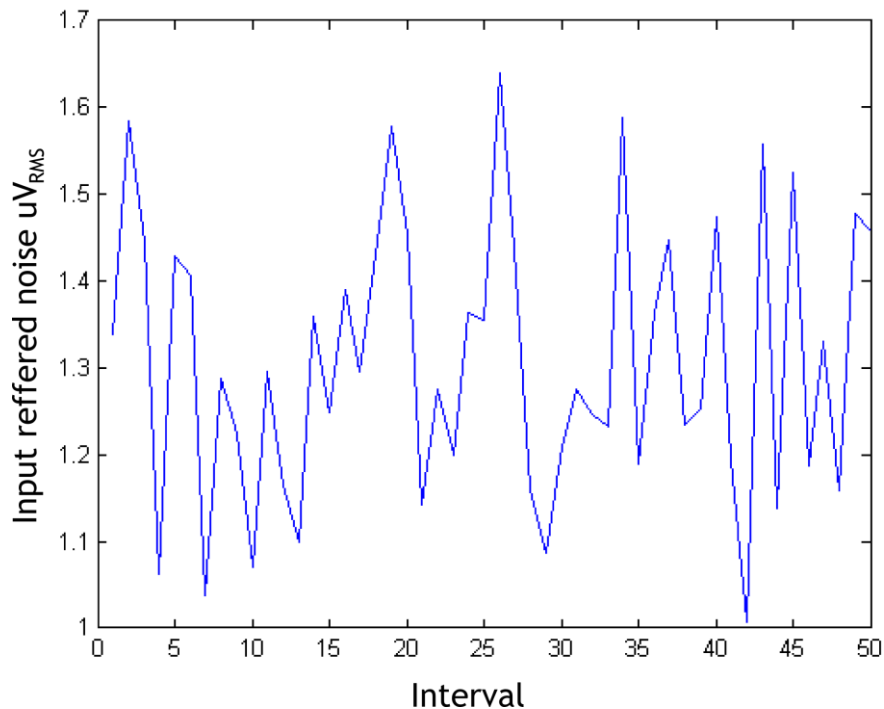


Figure 4.3 Input referred noise for 50 consecutive intervals lasting 1 ms each for a gain of 98.93 dB, measured to extract the worst case scenario on a series of measurements.

4.2 Biological Testing: Recording and Stimulation of Action Potentials

In the previous section we demonstrated how the system we designed and built met the initial specifications from an electrical point of view. However the final objective

for this work is to develop a system capable of both recording and stimulating neural activity. We therefore must perform biological experiments to validate the design and prove the system utility from the biological side. In both cases we used the reduced version of the system which features 2 channels for recording and 1 channel for stimulation.

4.2.1 Testing the Recording Electronics

The recording electronics were tested at Dr. Pancrazio's neuroscience laboratory at George Mason University, Fairfax, VA. We recorded the extracellular activity of an *in-vitro* primary neuronal culture which was the perfect test for our system's recording capability. The cells were obtained by enzymatic dissociation of cortical tissue on day-17 from an embryonic mouse. The method has been described in [54], [55] and [56]. The cells were plated on a microelectrode array (MEA) and they were allowed to form a mature neural network for 21 days prior to testing for spontaneous neural activity [54]. The 64-electrode MEA, with a 10 μm diameter for each electrode and an inter-electrode spacing of 200 μm , was purchased from Multichannel Systems (MCS, Germany).

The cells used in these measurements showed spontaneous electrical activity and they did not need to be stimulated in order to fire action potentials (APs). During recording the culture was kept at a constant temperature and the electrodes pads were contacted through probe station heads to our system. During recording the gain of our electronics system was set to 8000, and the output of our system was recorded using a commercial tool (Axon DigidataTM 1440A Data Acquisition System, Molecular Devices, CA) and processed on the PC using a dedicated software tool (Axon Clampex 10.3, Molecular Devices, CA).

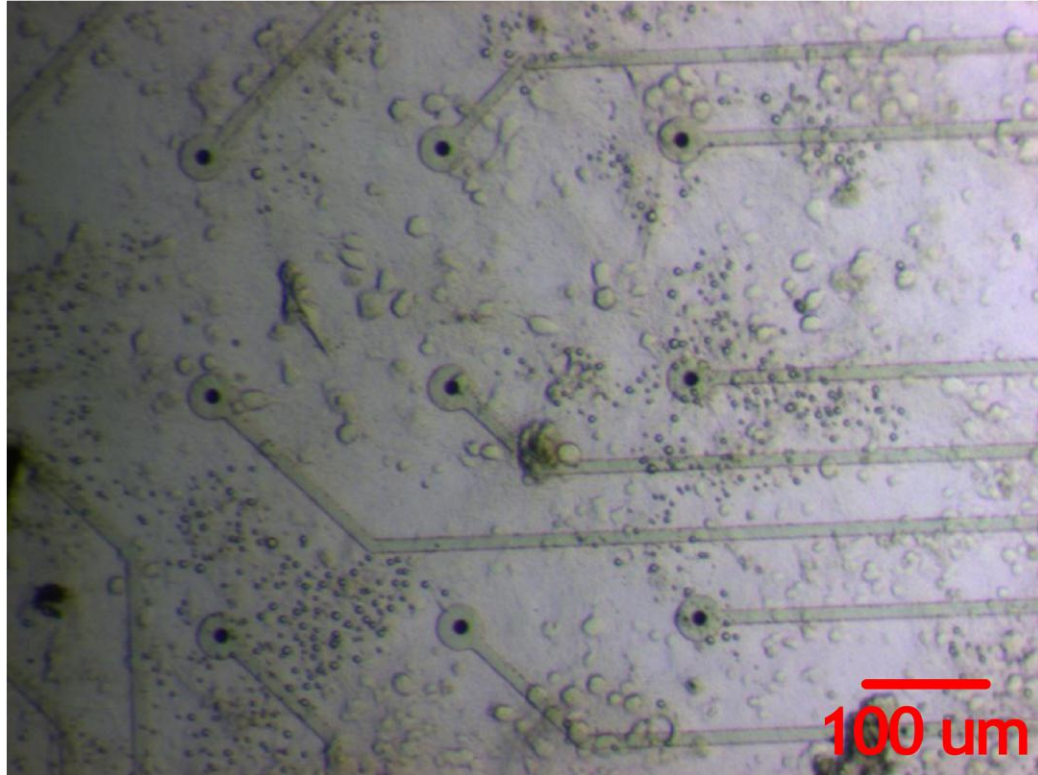


Figure 4.4 Photograph of neurons plated on the MCS MEA for extracellular recording at GMU. Courtesy of Dr. J.J. Pancrazio and Hamid Charkhkar, GMU Biomedical Engineering Department.

Figure 4.5 shows auto generated neural bursts on electrode 33 of the MEA. As can be seen from Figure 4.5(B) and Figure 4.5(C) the neural recording is repeatable in time and the two recording from the same type of cell activity give a very similar result.

Figure 4.6 shows three examples of action potential recordings from channel 33 of the MEA spaced in the time of a few seconds. The single action potential has an amplitude of about 500 mV after 8000 V/V of amplification and an average duration of up to 400 μ s.

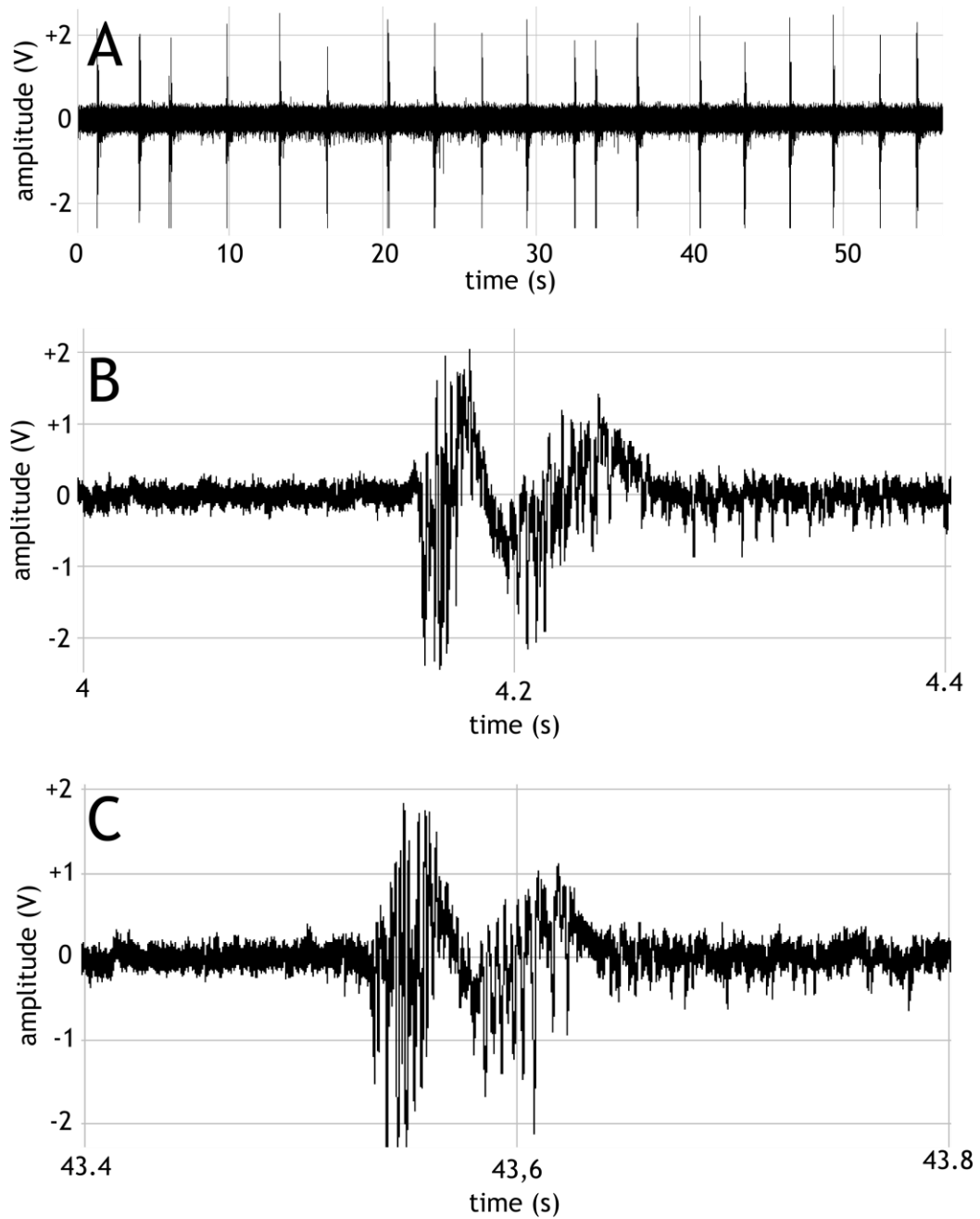


Figure 4.5 Spontaneous neural burst activity from the cells on electrode number 33. A: recording over a time of 60 s; B and C show detailed views of two bursts from the same electrode to show that these are indeed repeatable waveforms.

As a final test and validation of our electronics, the system was connected in parallel, to the same electrode, with a high-end commercial system (Plexon OmniPlex™, Plexon, Inc., TX). The gain was set to 8000 for both systems. The outputs of the two

systems were acquired, as in the measurements described above, with an Axon Digidata™ 1440A Data Acquisition System (Molecular Devices, CA) and stored using the data acquisition software Axon Clampex 10.3 (Molecular Devices, CA).

Figure 4.7 shows the two lines of acquisition with the upper trace being that from our custom system and the second one being the commercial tool. We noted that the commercial system and our system show a very similar signal shape, but the commercial tool has a delay of about 200 ms compared to our recordings.

Action potentials A and C from our system's recording and the same action potential from the commercial system, B and C, respectively, are highlighted and the image shows an impressive similarity (see Figure 4.7).

The reader can note that the commercial system has a lower noise level, meaning that future versions of our custom electronics must have improved noise performance in order to over perform on this feature.

4.2.2 Testing the Stimulation Electronics Module

In order to prove the validity of our architecture for both recording and stimulation, we have successfully tested the pulse generation unit to achieve burst neural activity. First, a C57BL/6J hippocampal slice was obtained and found to be capable of long term potentiating (LTP) using commercial tools (A-M Systems Model 1800 amplifier and 2200 isolation stimulator; Digidata™ Model 1440A low-noise data acquisition system).

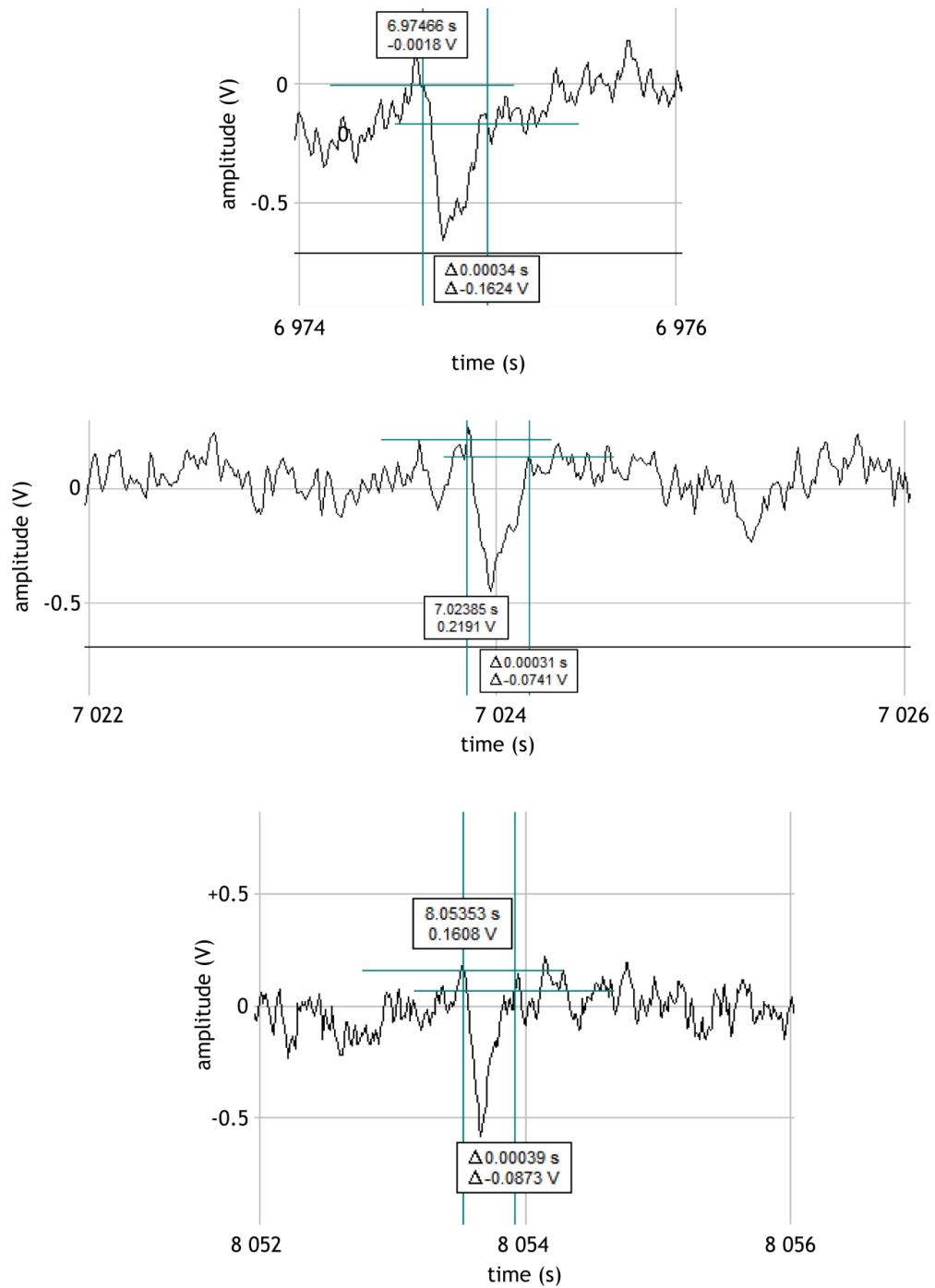


Figure 4.6 Single action potential recordings on electrode 33, gain set to 8000 V/V. Three recordings are displayed which demonstrates the repeatability of our system.

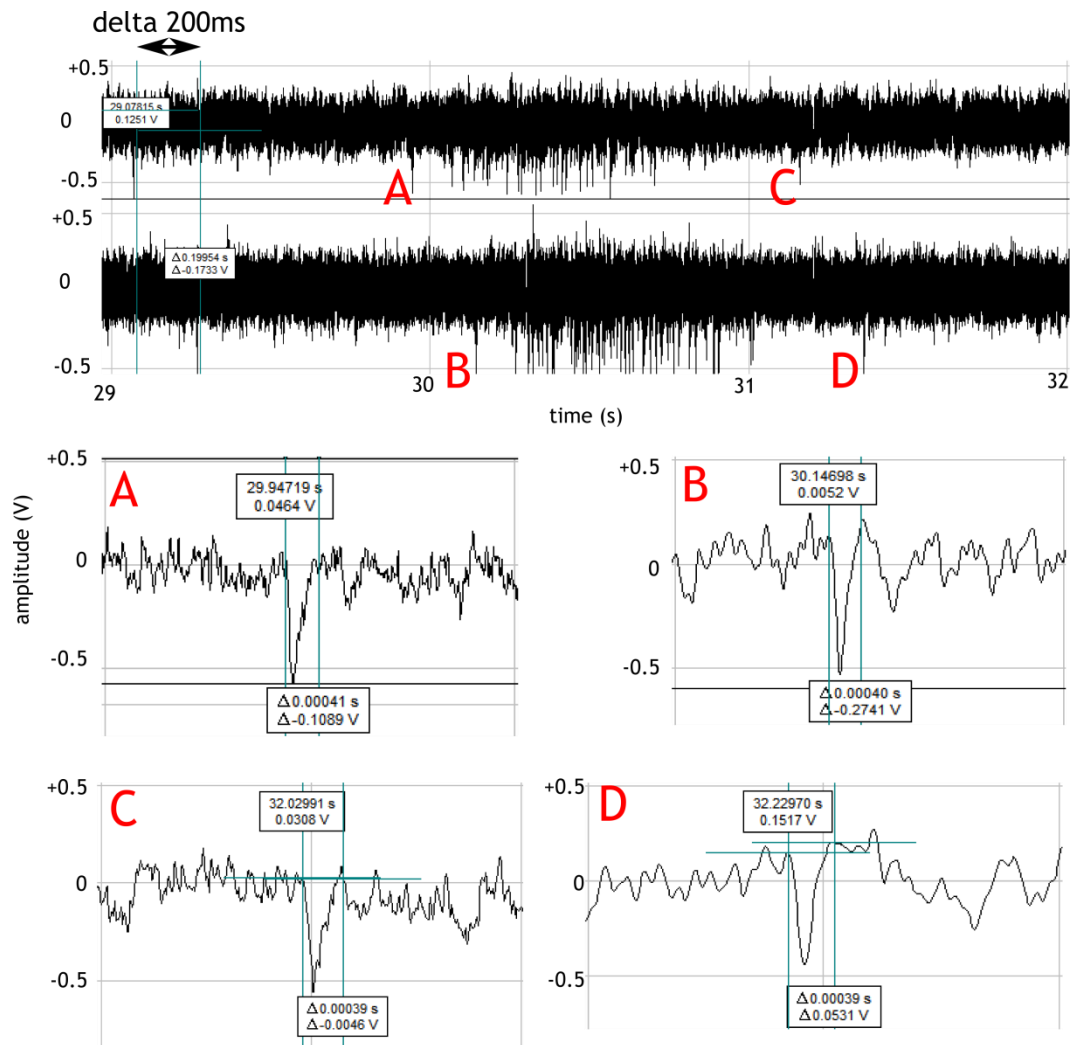


Figure 4.7 A comparison between our custom electronics (top trace plus A and C) and a commercial recording instrument from Plexon (bottom trace plus B and D). For time reference on the detailed images A - D please refer to the measurement boxes contained in the figure.

After that, we detached the stimulation electrode pair from the AM-Systems Model 2200 and connected to our stimulator. We connected a Tektronix TDS 1002B Digital Oscilloscope to the output of the Digidata Model 1440A. A 100 Hz bi-phasic stimulation pulse was applied from our stimulation system to the CA2/3 Schaffer's collaterals in the hippocampal slice and subsequent field excitatory post synaptic

potentials (fEPSPs) in the CA1 stratum radiatum were received and recorded by the Tektronix oscilloscope 1002B using the A-M Systems Model 1800 as amplifier.

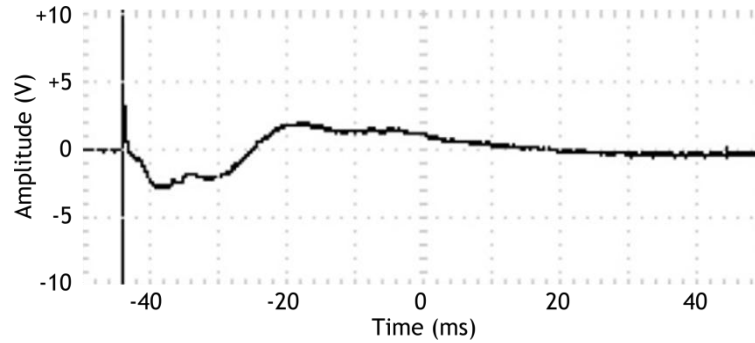


Figure 4.8 fEPSP CA1 hippocampal response induced by the stimulation circuit. The response is amplified 1000 times (horizontal resolution: 10 ms/div , vertical resolution: 5V/div, offset: 0V).

When using our system for recording we noticed that after the pulse reaches the LNA input, the output remained in saturation for a long time, on the order of tens of milliseconds, due to the slow time constants of the system. While this effect is negligible for pulses below ± 1 V, the artifact control for high voltage pulses had yet to be solved and a more detailed description of the problem will be provided later on in this Chapter.

Figure 4.9 shows the output response of the amplification channel when a ± 1 V biphasic pulse was applied. After the pulse ends, the output remains in saturation for about 1 ms, after which time it is ready to record data again. Thus the recording system is effectively blind for 1 ms after the stimulation has ended.

As the pulse amplitude increases, the time that the output takes to restore from saturation back to regular working conditions grows and the system becomes unusable for this kind of experiment. In the next Chapter a possible solution is proposed to resolve this issue in the near future.

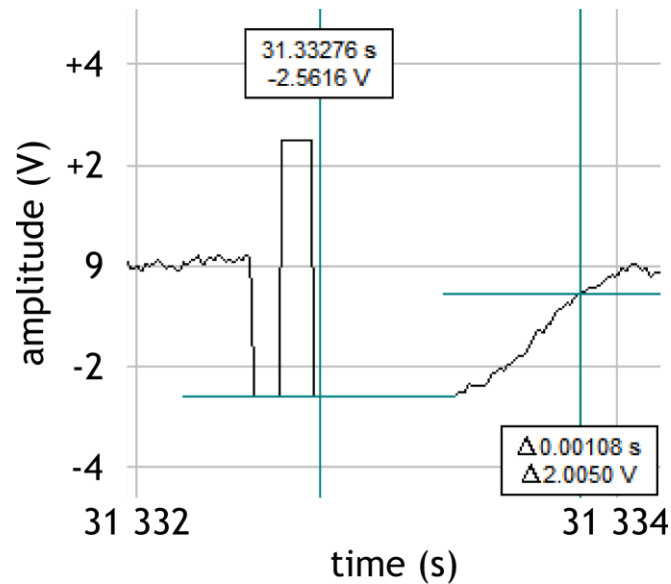


Figure 4.9 The output response of the amplification channel for a biphasic ± 1 V stimulation pulse at the input. Note that a 1 ms delay in recording occurs to saturation of the amplifier chain by the stimulation pulse.

4.3 Summary

After designing and simulating the architecture that we proposed, we realized a reduced 3 channel version of the system to characterize it electrically and to validate the architecture via *in-vitro* MEA measurements. Validation of the design will now allow us to complete the assembly of the full 64 channel system (composed of four (4) 16 channel modules) so that a full MEA stimulation and recording capability will be available to the USF SiC Group.

Using a simple set-up made of a function generator and an oscilloscope we characterized the electrical performance of our system, which features 98.83 dB gain over the 14 Hz 13 kHz band. These characteristics were superior to the commercial systems tested at George Mason University and clearly show one major advance that has resulted from this dissertation research.

The input referred noise is $1.6 \mu\text{V}_{\text{RMS}}$, which is higher than the value expected from simulation but significantly lower than the $3.5 \mu\text{V}_{\text{RMS}}$ posed as the upper limit from the specifications. The deviation from the expected value may be from both the non-realistic PSpiceTM device models that we used and the contribution of the environmental noise at the system input. The later problem can be rectified with proper electronics packaging and shielding which will be incorporated into the final system assembly in the near future.

After the electrical characterization we performed *in-vitro* measurements of action potentials from cultured cells plated on top of a MEA demonstrating the capability of acquiring neural activity. Moreover we connected our system in parallel to the same electrode with a high end, well-known commercially available dedicated tool in order to benchmark our system, and we found out that the two recordings were extremely similar. Our system outperformed the commercial tool on the delay between the action potential and the output available at the end of amplification chain with about a 200 ms timing difference. However the commercial system displayed a better noise performance, most likely from better electronics packaging and shielding and also from the lower bandwidth of their system which reduces the noise spectra in their system compared to ours.

Lastly we tested the system for the stimulation of neural activity and we were able to fire an action potential from a mouse hippocampal brain slice. Unfortunately, while when using both our stimulation and recording system together, we recognized that for stimulation pulses over $\pm 1 \text{ V}$ of amplitude artifacts appeared at the output of the amplification chain that make the system blind for several milliseconds. This issue has to

be resolved in the future in order to be capable of sending ± 50 V biphasic pulses while being able to record almost instantaneously from the same electrode.

CHAPTER 5: CONCLUSIONS AND FUTURE WORKS

Brain computer interfaces are an extremely important field of research that has evolved very far in the last few decades, bringing to the scientific community a large amount of systems for both *in-vitro* and *in-vivo* applications. The way they work is straightforward and complex at the same time: different parts of the human and the animal body communicate with each other by means of electrochemical pulses called action potentials that can be transmitted by a large variety of electrically active cells available in our body.

The capability of controlling, understanding and generating such signals, could lead to huge progress in both medicine and engineering, in particular for many current patients who have mobility limitations and diseases, such as paralysis, blindness, etc. Next generation prosthetics with sensing capabilities could find a definitive cure thanks to advances in this field of research. A complete understanding of all the mechanisms that regulate these processes is pretty complex and is the result of an interdisciplinary effort to fill the gap between the worlds of biology and engineering, called neuroengineering in this case

In Chapter 1 an overview of different systems used to interface electronic systems and electrically active cells was presented, that showed that concrete steps have been made in many areas of this field. Systems have been presented that are capable of restoring communication between two neurons not in contact with each other, to stimulate brain activity by means of non-invasive light pulses, to study an extremely large

population of cultured cells using a 16000+ array of electrodes individually read to acquire neural activity, and other impressive advances in the field. Some of these systems aim to just record neural activity, while others present both recording and stimulation capabilities.

While all of these systems are different in terms of both their functionality and objectives, all of them show a common characteristic, the most important material for their realization is silicon. Silicon is an easy choice because it is largely available for fabrication, is cheap and its characteristics are well-known across the scientific community. Unfortunately the first chapter discussed how it has been proven that silicon based devices implanted in the body fail after months of implantation and that there is a strong need for a material that features the main advantages silicon, i.e. the fact that electronics can be realized on board in very close proximity to the recording site, and that at the same time can be implanted for long times in the human body. In this work we presented a custom system the over performed a commercial tool in terms of performance and flexibility, allowing a very high degree of flexibility as electrodes realized in new materials are available for testing.

The most important part when designing a system for neural data recording and stimulation is the *analog front end* which determines the main electrical characteristics of such a tool: electrical impedance, bandwidth, gain and input referred noise. The most popular approaches have been analyzed and their electrical characteristics have been listed, but none of them could completely fulfill our requirements, in particular we needed a way to withstand high voltages up to ± 50 V pulses while featuring a high impedance to ensure a stable and repeatable recording capability.

5.1 System Design and Electrical Testing

We designed our custom electronics from the ground up based on the passive high pass input stage in Chapter 2, together with a stimulation circuit to provide both recording and stimulation capabilities. Chapter 2 included a detailed description of all the different modules of the bi-directional electronics system, both analog and digital, that together compose the system. The system designed features 64 channels of stimulation and acquisition divided into 4 modules of 16 channels each. This modular approach enables a great degree of flexibility because the system can be expanded by adding more and more modules without having to redesign the full electronics system. Each channel presents a protection circuit that withstands high voltage pulses and, due to its Darlington architecture, increase notably the input impedance. A *LNA* is based on a high pass filter and a non-inverting operational amplifier configuration that provides a gain of 46 dB to the signal. This stage is fundamental for the noise performance of the system and the operational amplifier that we used is a world class leading low noise device. We added to the amplification chain a second order low pass filter to increase the filtering efficiency in the frequency range of interest, i.e. 20 Hz to 10 kHz, while reducing aliasing during the successive digital sampling. Finally the signal goes through a *VGA* to be further amplified for a total gain that can span from 61 to 100 dB. After amplification the 16 channels from each module are time domain multiplexed to a unique channel and sampled by an *ADC* that works at a sampling rate of 1 Msps, so that each channel is sampled at 62.5 ksps, i.e. almost 6 times the signal bandwidth.

In order to validate the architecture described above we realized a 3 channel prototype and measured the electrical characteristics of the single stages that form the

amplification and filtering stage. The results were extremely positive. We measured a variable software programmable gain that can be set between 61 and 99 dB over a frequency range of 18 Hz to 12 kHz. This complies perfectly with the kind of signal that we intend to acquire that spans from a few tens of hertz up to 10 kHz.

The most important result was that the input referred noise voltage was as low as $1.6 \mu\text{V}_{\text{RMS}}$ when integrated over a 25 kHz bandwidth. This extremely low value enables for good recording quality and SNR even for higher gain operation.

5.2 Biological Measurements and Performance Comparison

Beside the electrical test and characterization the real validation for a tool like the one we realized is the recording of neural activity from electrically active cells. In Chapter 4 we reported on measurements performed at Dr. Pancrazio's laboratory at George Mason University, Fairfax, VA. Our system was capable of recording neural activity from spontaneously firing neural cells plated on a *MEA*. We recorded both firing burst, i.e., a large number of action potentials in rapid sequence, and single action potentials from the plated cells.

The system was then connected in parallel to the same recording electrode with a commercially OmniPlexTM available tool (Plexon, CA) for *MEA* recording and the two recorded traces were compared. Not only was the quality of recording very similar to each other, but our system outperformed the commercial instrument in terms of the latency between the instant the action potential passes close to the electrode and the moment the recording channel is available at the output of the system. Being that the commercial tool is one of the best and most expensive in commerce (more than \$70 k for

only the recording unit for 64 channels) it was a very significant test bench for performance evaluation and our system did extremely well.

5.3 Design and Biological Test of the Stimulation Circuit

In addition to the recording electronics, we designed and realized a stimulation circuit capable of sending high voltage biphasic pulses on a two wire channel that is floating with respect to the fluid reference voltage. The pulse shape and amplitude can be varied via software giving a great degree of flexibility. We tested the stimulation circuit to demonstrate that it is able to induce neural activity, which it did. Using a hippocampal brain slice from a wild type mouse at the Byrd Institute (University of South Florida) we connected a standard commercial tool described in Chapter 4 to make sure that the slice was active and responsive. Once we were sure of the tissue slice's electrical activity, we disconnected the commercial system and connected our stimulator, obtaining the exact same hippocampal response after stimulation with a pulse of ± 5 V.

5.4 The FPGA Control Unit

In order to control all of the different analog and digital devices that form the system we wrote a massive amount of code for an FPGA based development board (Digilent Atlys) that enables: gain setting of all the channels at once, stimulation pulse duration and amplitude, channel selection at the *ADC* input, data acquisition from the *ADC*, filtering, data packaging and transmission over a standard Ethernet connection to a PC for persistent storage and post processing. For this reason a Java[®] driver was realized to capture *UDP* packets and store the data in a *CSV* file. The data transmission system was tested for different times and no data loss was experienced over a point-to-point line.

5.5 What Is Next?

5.5.1 From the Prototype to the Full 16 Channel Board

The current prototype used for the validation of the system featured two recording channels and one stimulation channel. The next step will be the realization of the actual 16 channel board featuring, in addition to the analog section, the multiplexer and the *ADC* for signal acquisition.

The last changes in the architecture due to modifications necessary during system test and debug will be inserted in the schematic and added to the PCB layout. The final board is made up of around 600 different components and will be sent out to a commercial vendor for assembly.

The final layout and module organization will be then be defined and it will determine the interconnection strategy of the four 16 channel modules with the FPGA control unit.

5.5.2 Design of a Custom ± 50 V Voltage Regulator

Based on the author's knowledge, there are no commercially available linear voltage regulators able to provide voltage regulation at levels as high as ± 50 V. In particular the most relevant devices we found are the LM317 and LM337 variable linear regulators. Their maximum voltages are respectively +37 V and -37 V.

Due to the fact that our system features a very high gain of 100 dB, it is very sensible to noise and, in particular, a poor power supply line can cause the output to oscillate and be completely unusable. In order to increase the *power supply rejection ration (PSRR)* and to solve this problem we had to add a dual stage of regulation on all the power supply lines in the following order: ± 50 V and ± 2.5 V. Due to this limitation,

currently our maximum possible operating voltage is ± 35 V instead of the ± 50 V required from system specifications.

While this is not a major limitation for the vast variety of electrode materials and cells/tissue slices, it could be a problem while testing new and different materials that, for example, can feature very high resistive paths from the stimulation node to the electrode, thus requiring very high voltages at the beginning of the chain to have enough power at the electrode site.

In this case a custom bipolar linear voltage regulator has to be designed and realized with a variable or fixed output of ± 50 V and a *PSRR* of at least two times the nominal value of the *LM317* and *LM337* for a total required *PSRR* of at least 160 dB on both the positive and the negative power supply lines.

5.5.3 Capacitive Coupling Between the Stimulation Circuit and the Recording Unit

The biphasic stimulation pulses consist of a differential signal with the *STIM⁺* line that can be connected to any of 8 electrodes on each 16 channel module, while the *STIM⁻* can be connected to any of the remaining 8. These two signal lines are completely floating with respect to the fluid reference, which is also the reference voltage of the single ended inputs of the amplification stage.

Even if not directly connected by any wire or *PCB* trace, the *STIM⁺* and *STIM⁻* connections have a conductive return path through the system reference voltage and the channel input through the conductive solution where the cells are cultured.

During our first electrical tests of the system we noted that a remarkable 50/60 Hz cross talk was present between the stimulation section reference voltage *STIM⁻* and the

recording unit. This crosstalk signal caused the output of the recording chain to oscillate between positive and negative saturation.

The cause of such a problem was the fact that the two transforms used to generate the power supply lines for the recording unit and the stimulation unit, respectively, presented a notable capacitive coupling between their primary windings (connected in parallel to the wall outlet) and their secondary windings that theoretically had to be completely floating with respect to each other.

Differences in manufacturing processes and dimensions caused this effect to be very evident. We could distinctly observe a 1 V_{PP} stationary 50/60 Hz noise between the two secondary windings.

Currently the only way we found to avoid this destructive cross talk is to power the stimulation circuit by means of batteries, but this limitation must be overcome in order to perform long term experiment of days or weeks.

We recently discovered that there is in the market a special class of transformer that features a very high isolation between the primary and secondary windings. This could be a possible solution to the problem, but tests have to be performed in order to understand if this is a viable solution.

Alternatively a different architectural approach can be investigated made of active components to limit the crosstalk between the two reference voltages.

5.5.4 Blind Time After Stimulation Pulse

As we reported in Chapter 4, after a stimulation pulse reaches the input electrode of the amplification chain, due to the very high gain adopted in this system, it causes the input stages to saturate and, after the pulse ends, it can take a long time for the system to

recover to the regular recording conditions. Due to the large time constants needed to work at low frequency, such a recovery time can be as long as tens of milliseconds and this is clearly not acceptable because action potentials can occur as fast as 1 ms after to stimulation pulse ends.

This is a major problem in this kind of system and there is a large variety of solution proposed to solve this problem. However, even with our new knowledge and from tests made on the electronic board with different possible approaches, there is not a definitive solution yet.

Figure 5.1 shows the equivalent electrical circuit model of the *LNA* input. *M1* is a MOSFET switch and is driven by the FPGA control unit. *M1* is closed during stimulation to keep the *LNA* input a 0 V and is opened just after the stimulation pulse to let the signal propagate through the amplification chain.

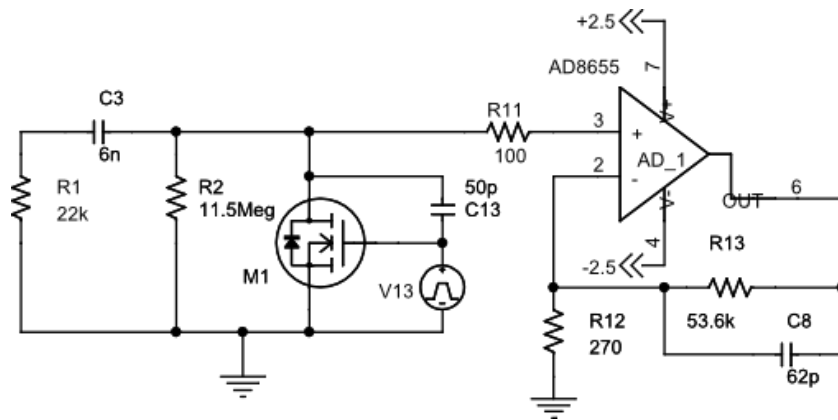


Figure 5.1 The AFE input stage electrical equivalent circuit model and was simulated with PSpice™.

Figure 5.2 shows the moment when the switch *M1* changes state from high (switch closed) to low (switch open). A parasitic capacitive coupling is present, especially when using *off-the-shelf* components instead of integrated circuits, which is

modeled by the 50 pF capacitor *C13*. When the signal, modeled by the pulse generator *VI3*, commutes from high to low amplitude this brings the node *C3-R2* to negative value, ideally to -2.5 V. When the signal reaches about -0.7 V, the intrinsic diode of the MOSFET *M1* switches ON and clamps the node at that value. Once the transient of *VI* is over, the capacitance *C13* has to discharge from -0.7 V through the large resistor *R2*, with a long time constant ($\tau=RC$) of 70 ms which results in the wave form shown in the bottom of Figure 5.2 at the output of the *LNA*.

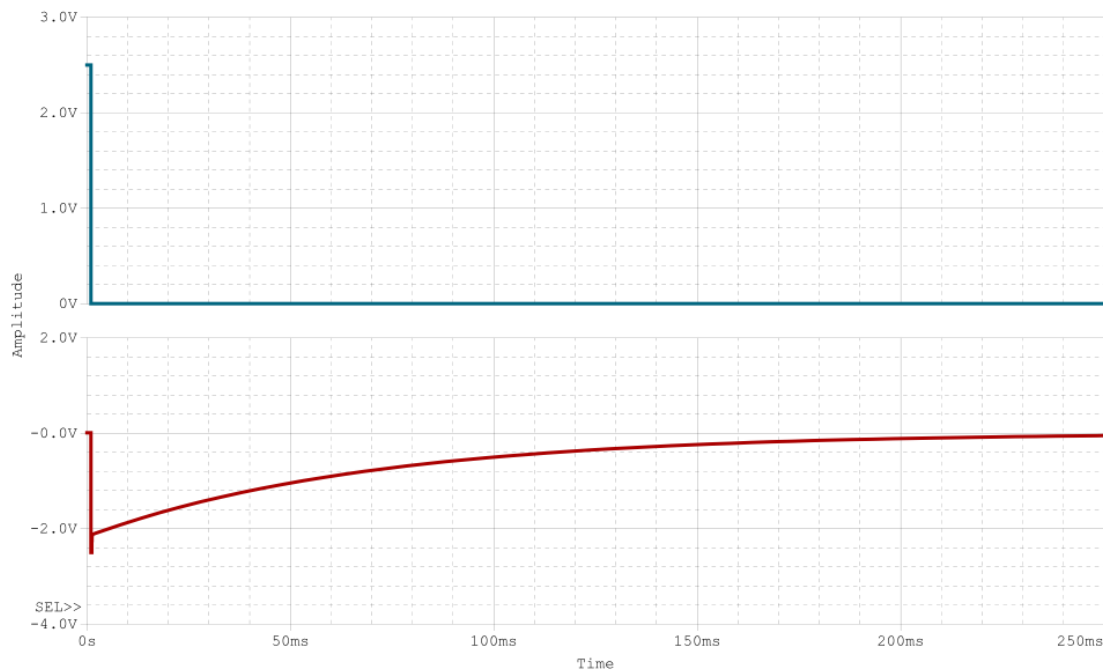


Figure 5.2 Simulation of the blind time in the amplifier chain after the stimulation pulse has been applied. Upper plot - the signal that drives the MOSFET switch *M1*. Lower plot - *LNA* output which is recovering to its normal resting condition of 0 V very slowly (over hundreds of milliseconds).

In order solve this problem and limit the blind time to a maximum of 1 ms, we propose the solution shown in Figure 5.3. After the switch is opened and the system follows the natural (slow) evolution to 0 V through *R2*, a charge pump (formed by *C9*,

$D1$ and $D2$) injects a very low amount of charge into $C6$ at each transition of the charge pump driving signal, to help speed up the system recovery to reach 0 V. The charge pump circuit is ON only when the output of the comparator $U1$ detects a negative voltage at the LNA input. The LNA input is filtered ($R14$ and $C10$) to reduce the switching noise from the charge pump.

Using this technique we are able to recover the LNA input and output to almost 0 V in less the 1 ms. Figure 5.4 shows the simulated evolution of the signals as a function of time.

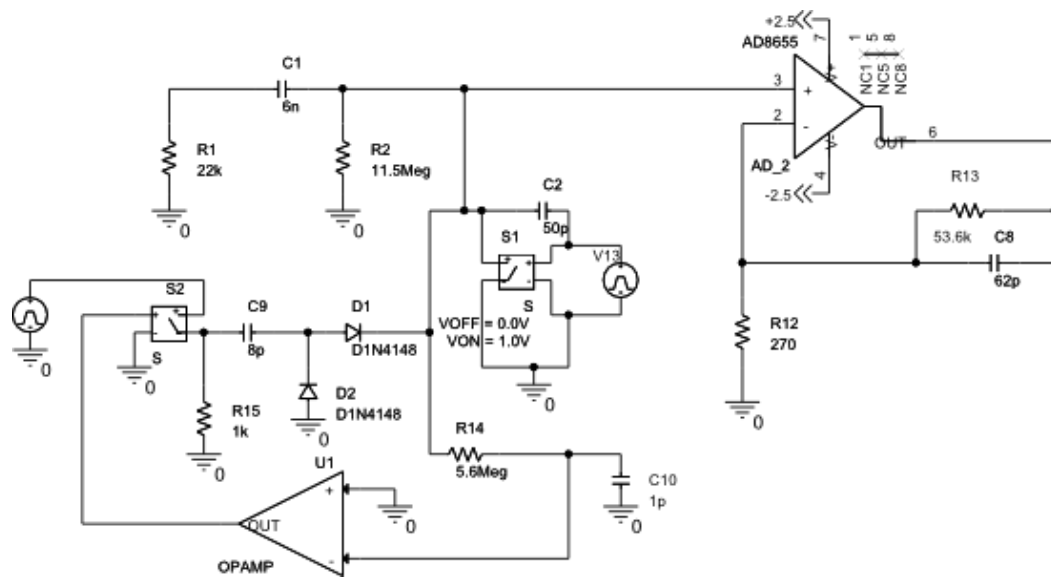


Figure 5.3 The proposed circuit to reduce blindness time after voltage stimulation. $C9$, $D1$ and $D2$ form a charge pump which should reduce the blindness time to acceptable levels.

The LNA input, and thus its output, are forced to 0 V by the charge pump that charges $C1$ in less than 1 ms. The process is self-controlling and automatically ends when the node under control, in this case the LNA input but it can be any other node, like the LNA output, reaches a 0 V value.

At this time this architecture has only been simulated. In order to validate this approach, a real prototype of the circuit will be realized and the actual performance evaluated.

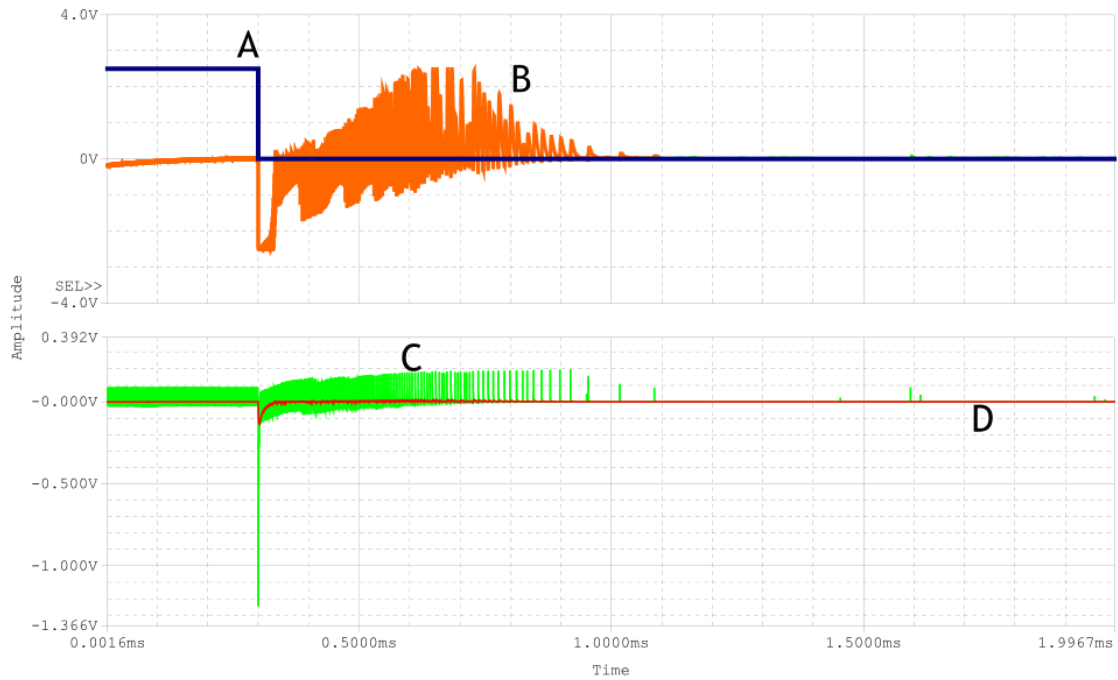


Figure 5.4 The simulated evolution of the *LNA* output using the proposed stimulation artifact suppression circuit. (A) the signal that drives the switch *SI*, (B) the output of the *LNA*, (C) the input of the *LNA* and (D) the filtered input of the *LNA*. The resulting blindness time is estimated to be ~ 1 ms with this circuit which is more than adequate to enable bi-directional communication with our system.

5.5.5 Neural Recording Using from Silicon Carbide MEA

A 3C-SiC MEA has been designed and fabricated within the Silicon Carbide group at University of South Florida using Au electrodes on lightly-doped 3C-SiC grown on (100)Si. Silicon Carbide, as explained in Chapter 1, is a promising material for the manufacturing of the next generation of implantable devices because it features both a

high degree of biocompatibility in the neural environment and the capability of building *on-board* electronic circuitry for signal processing and conditioning.

In the future we want to test our system with this advanced 3C-SiCMEA in the exact same way that we measured neural activity in the *in-vitro* experiment to validate the system (Chapter 4).

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APPENDICES

Appendix A Electric Schematics

In this section schematic circuit diagrams and PCB layout masters are presented of all the different modules of the system. A connection scheme and numbering of all the control signals and power lines is also presented to complete the information about the platform.

Appendix A (Continued)

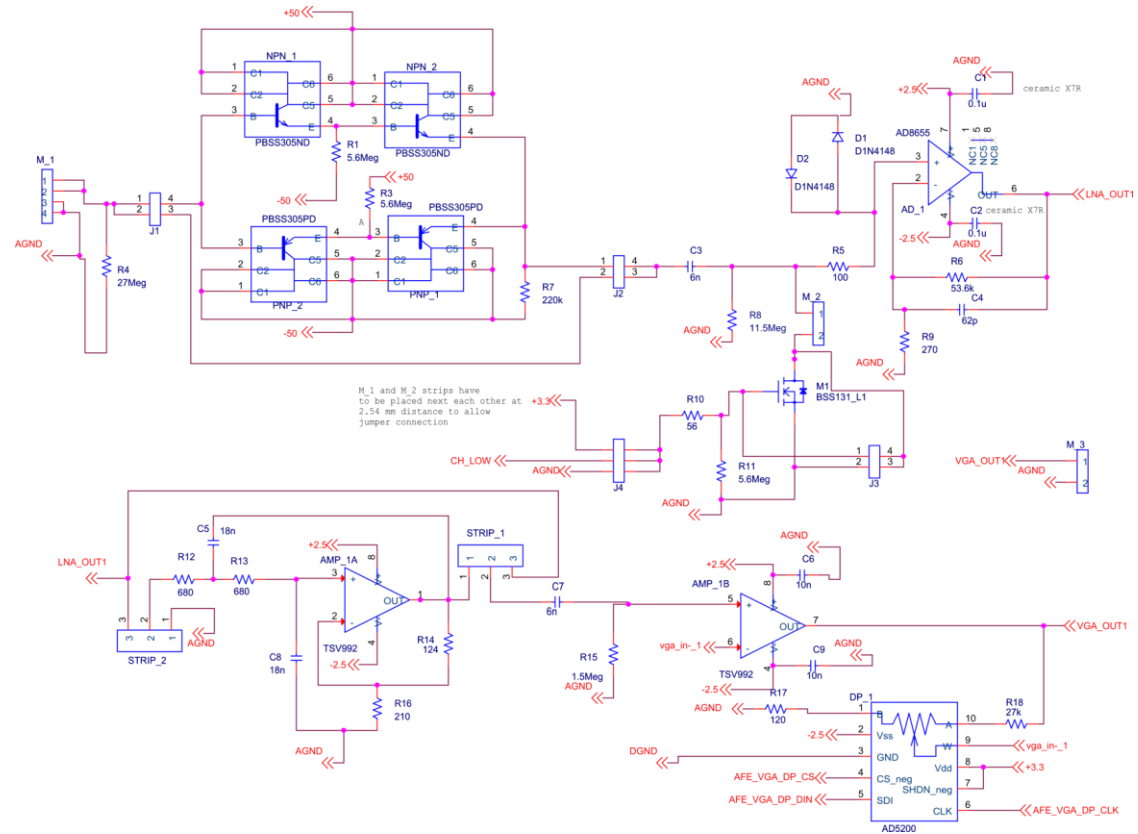


Figure A.1 Circuit schematic of a typical channel from the electrode interface to the VGA output.

Appendix A (Continued)

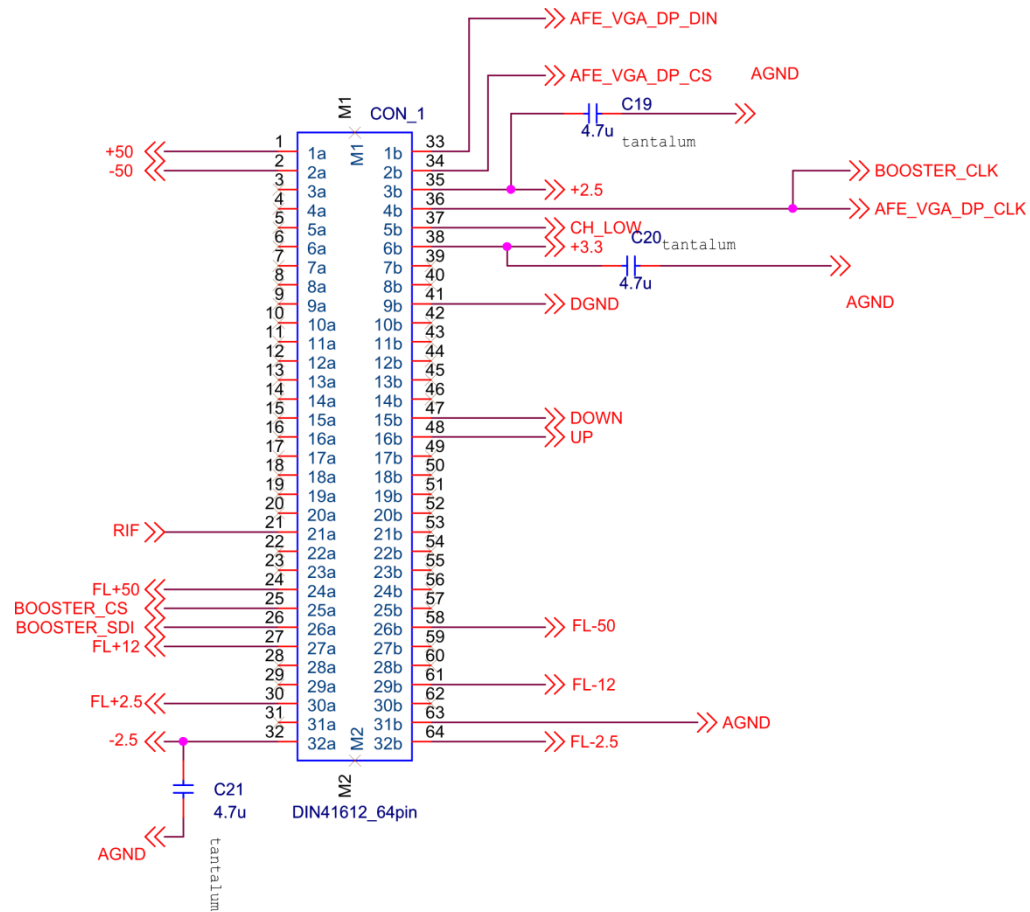


Figure A.2 Connection diagram of the DIN41612 connector for digital data interfacing and power supply lines.

Appendix A (Continued)

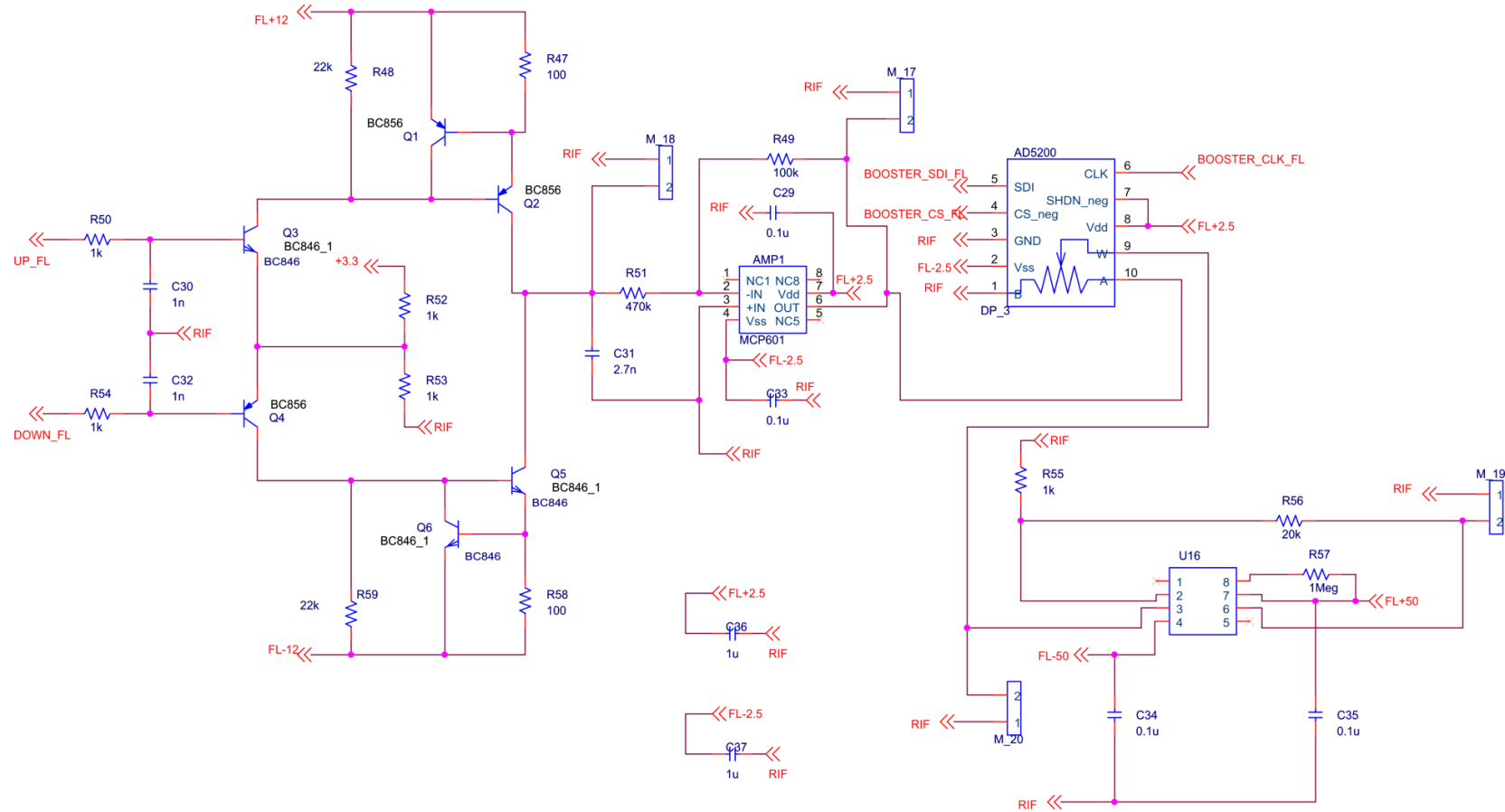


Figure A.3 Circuit schematic of the stimulation unit

Appendix A (Continued)

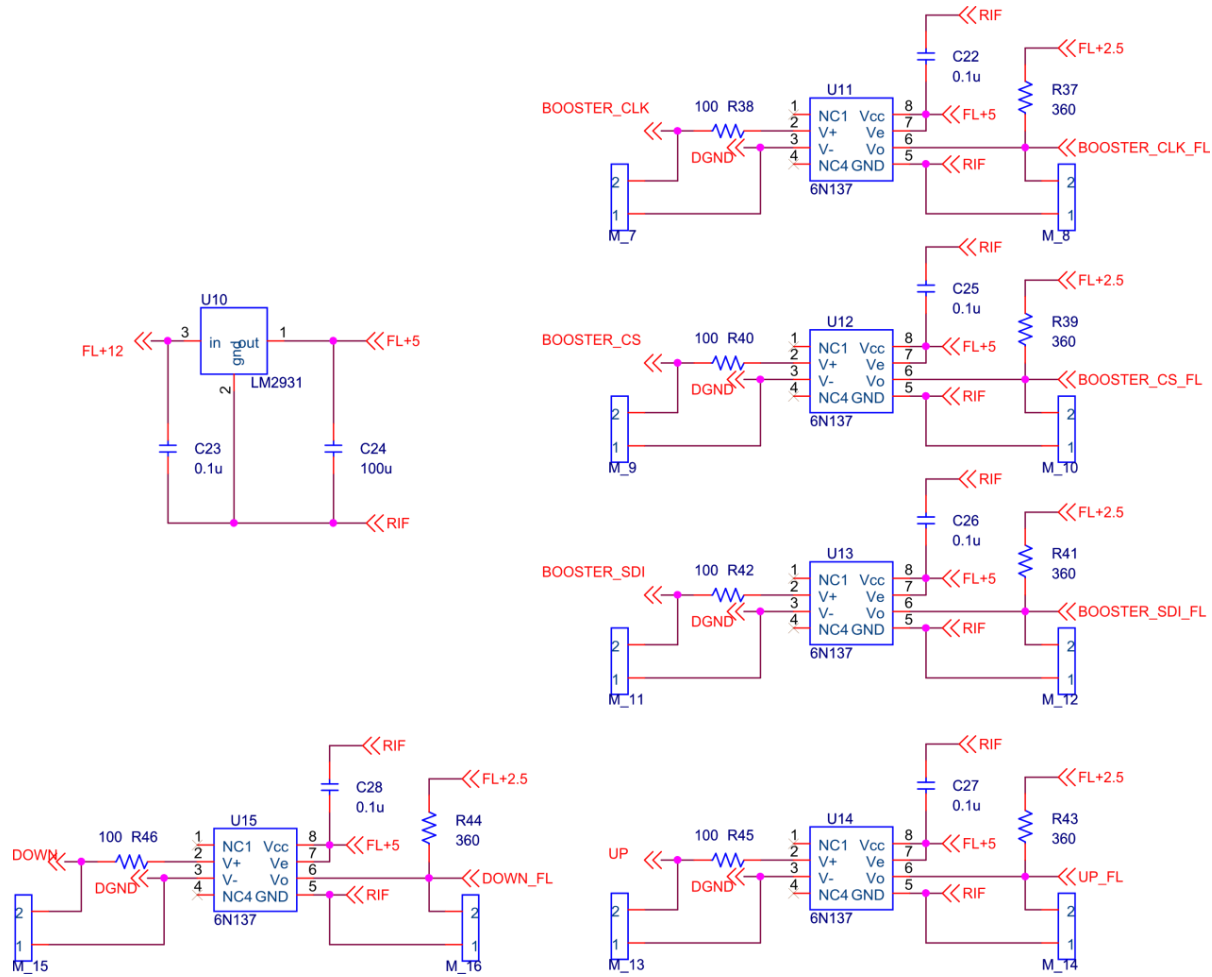


Figure A.4. Schematic diagram of the opto-isolation stage to connect the floating stimulation circuit digital signals to the FPGA.

Appendix A (Continued)

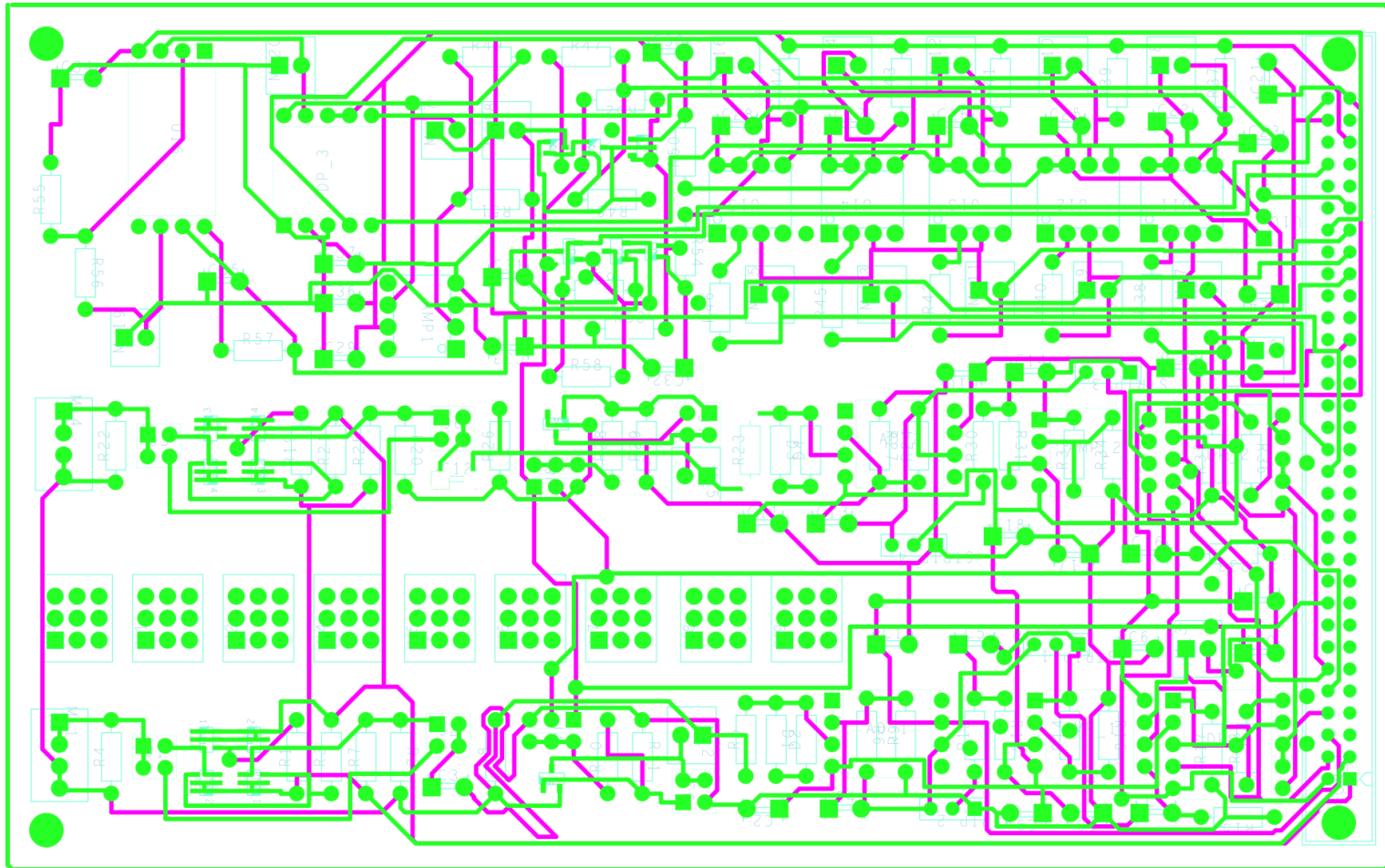


Figure A.5 Top (green) and bottom (purple) layer of the PCB circuit layout

Appendix A (Continued)

Name	Description	VHDCI	VHDCI COLOR	AFE1	AFE2	AFE3	AFE4	Booster	Power supply	Resistor	Port
AGND		NC		63	63	63	63	63	63		
DGND		42	Yellow	41	41	41	41	41	41		
RIF		NC		NC	NC	NC	NC	21	21		
FL+50		NC		NC	NC	NC	NC	24	24		
FL-50		NC		NC	NC	NC	NC	58	58		
FL+12		NC		NC	NC	NC	NC	27	27		
FL-12		NC		NC	NC	NC	NC	61	61		
FL+2.5		NC		NC	NC	NC	NC	30	30		
FL-2.5		NC		NC	NC	NC	NC	64	64		
+3.3		NC		38	38	38	38	38	38		
+2.5		NC		35	35	35	35	35	35		
-2.5		NC		32	32	32	32	32	32		
+50		NC		1	1	1	1	1	1		
-50		NC		2	2	2	2	2	2		
AFE_VGA_DP_CLK	Digital Potentiometer Clock. 1 for all AFEs	29	Orange / Dark Blue	36	36	36	36	36	NC	R46	T6
AFE_VGA_DP_CS	Digital Potentiometer Chip Select. 1 for all AFEs	31	Dark Blue / Purple	34	34	34	34	34	NC	R49	R7
STIM_ZERO/VGA_LOW	Tells whether the stimulus output is above or below 0V	28	Orange / Dark Green	NC	NC	NC	NC	28	NC	R43	N7
EN_OPA	Enable the output of the OPA454	23	Grey / Bordeaux	NC	NC	NC	NC	29	NC	R35	M8
CH_LOW	Signal to drive the MOS that grounds the LNA input	37	Orange / Black	37	37	37	37	NC	NC	R8	V15
AFE_VGA_DP_DIN	Digital Potentiometer Data In. 1 for all AFEs	32	Dark Blue / Black	33	33	33	33	33	NC	R51	N6
A0_MUX	Gestione Mux, tutti Afe in parallelo	9		56	56	56	56	56	NC		
A1_MUX	Gestione Mux, tutti Afe in parallelo	10		55	55	55	55	55	NC		
A2_MUX	Gestione Mux, tutti Afe in parallelo	12		53	53	53	53	53	NC		
A3_MUX	Gestione Mux, tutti Afe in parallelo	13		52	52	52	52	52	NC		
EN_MUX	Gestione Mux, tutti Afe in parallelo	15		50	50	50	50	50	NC		
ADC_CLK	Clock ADC degli AFE, 1 per tutti	20		45	45	45	45	45	NC		
ADC_CS	Chip Select ADC degli AFE, 1 per tutti	22		43	43	43	43	43	NC		
ADC_SDATA_1	SPI data in canale 1	44		-					NC		
ADC_SDATA_2	SPI data in canale 2	46			-				NC		
ADC_SDATA_3	SPI data in canale 3	47				-			NC		
ADC_SDATA_4	SPI data in canale 4	49					-		NC		
PULSE_L1		NC		6	6	6	6	6	NC		
PULSE_L2		NC		5	5	5	5	5	NC		
MAX_AFE_CLR	MAX4800A clear, 1 per tutti gli AFE	34		31	31	31	31	31	NC		
MAX_AFE_LE	MAX4800A latch enable, 1 per tutti gli AFE	3		62	62	62	62	62	NC		
MAX_AFE_DOUT	MAX4800A sezione AFE DOUT	4		61	61	61	61	61	NC		
MAX_AFE_DIN	MAX4800A sezione AFE DIN	6		59	59	59	59	59	NC		
MAX_AFE_CLK	MAX4800A sezione AFE Clock	7		58	58	58	58	58	NC		
UP	Drive the booster UP	57	Grey / Dark Blue	NC	NC	NC	NC	48	NC	R36	N8
DOWN	Drive the booster DOWN	68	Grey / White	NC	NC	NC	NC	47	NC	R55	V5
BOOSTER_CS	CS for the booster pulse amplitude	25	White / Red	NC	NC	NC	NC	25	NC	R37	U8
BOOSTER_SDI	SDI for the booster pulse amplitude	26	White / Yellow	NC	NC	NC	NC	26	NC	R41	U7

Figure A.6 Connection scheme and list of all the control and power signals

Appendix B FPGA Firmware

Listed below is the FPGA VHDL code that realizes the functions of the recording module.

```
`timescale 1ns / 1ps
module top_module(
    input clk_100_pin,
    output PhyResetOut_pin,
    // input MII_TX_CLK_pin,
    output [7:0] GMII_TXD_pin,
    output GMII_TX_EN_pin,
    output GMII_TX_ER_pin,
    output GMII_TX_CLK_pin,
    input [7:0] GMII_RXD_pin,
    input GMII_RX_DV_pin,
    input GMII_RX_ER_pin,
    input GMII_RX_CLK_pin,
    output MDC_pin,
    inout MDIO_pin,
    output [7:0] leds,
    /* input sw,*/
    input [5:0] btn,

    output wire A0,
    output wire A1,
    output wire A2,
    output wire A3,
    output wire ClkADC/*,
    output wire CS_n,

    input wire SDATA1,
    input wire SDATA2,
    input wire SDATA3,
    input wire SDATA4
    */
);

assign leds[7:3] = btn[5:1];
//assign leds[0] = sw;

// System clocks
//wire clk_100;
wire clk_100_buf;

//Global Clock Buffer
IBUFG ibufg_100 (
    .I(clk_100_pin),
    .O(clk_100_buf));

// FSM reset generator
localparam RST_DELAY = 3;
reg rst = 1'b1;
reg [RST_DELAY-1:0] rst_dly = {RST_DELAY{1'b1}};
always @(posedge clk_100_buf)
    if (clk_125_tx_locked)
        {rst,rst_dly} <= {rst_dly,1'b0};
```

Appendix B (Continued)

```
// 125 MHz for PHY. 90 degree shifted clock drives PHY's GMII_TX_CLK.
wire clk_125, clk_125_GTX_CLK, clk_125_GTX_CLK_n, clk_125_tx_locked;
wire clk_150, pll_rst;
wire clk_50;

Clock4Generator clock4Generator(
    .clk_100_buf(clk_100_buf),
    .clk_125(clk_125), // 0 deg
    .clk_125_GTX_CLK(clk_125_GTX_CLK), // 90 deg
    .clk_125_GTX_CLK_n(clk_125_GTX_CLK_n), // 270 deg
    .clk_150(clk_150),
    .clk_50(clk_50),
    .RESET(pll_rst),
    .LOCKED(clk_125_tx_locked));

// PLL reset
// http://forums.xilinx.com/t5/Spartan-Family-FPGAs/RESET-SIGNALS/m-
// p/133182#M10198
reg [25:0] pll_status_counter;
//always @(posedge clk_100)
always @ (posedge clk_100_buf)
    if (clk_125_tx_locked)
        pll_status_counter <= 0;
    else
        pll_status_counter <= pll_status_counter + 1'b1;

assign pll_rst = (pll_status_counter > (2**26 - 26'd20)); // Reset for 20
cycles

//Drive the GTX_CLK output from a DDR register
OFDDRSE OFDDRSE_gmii_inst
    (.Q(GMII_TX_CLK_pin), // Data output (connect directly to top-
level port)
    .C0(clk_125_GTX_CLK), // 0 degree clock input
    .C1(clk_125_GTX_CLK_n), // 180 degree clock input
    .CE(1'b1), // Clock enable input
    .D0(1'b0), // Posedge data input
    .D1(1'b1), // Negedge data input
    .R(1'b0), // Synchronous reset input
    .S(1'b0) // Synchronous preset input
    );

// communication signals
wire [31:0] datain;
wire start_transmission;
wire ready_to_start;
wire destination_rdy;

wire [31:0] cntf_databus;
wire cntf_wr_en;

wire Amax;
wire start_acquisition, threshold;
wire [13:0] numero_quartetti;

wire rdy96_32;

//Ethernet module
```

Appendix B (Continued)

```
ethernet interfaccia_ethernet(  
    .rst(rst),  
    /* .duplex(sw), */  
    .PhyResetOut_pin(PhyResetOut_pin),  
    .GMII_TXD_pin(GMII_TXD_pin),  
    .GMII_TX_EN_pin(GMII_TX_EN_pin),  
    .GMII_TX_ER_pin(GMII_TX_ER_pin),  
    .GMII_RXD_pin(GMII_RXD_pin),  
    .GMII_RX_DV_pin(GMII_RX_DV_pin),  
    .GMII_RX_ER_pin(GMII_RX_ER_pin),  
    .GMII_RX_CLK_pin(GMII_RX_CLK_pin),  
    .MDC_pin(MDC_pin),  
    .MDIO_pin(MDIO_pin),  
    .clk_125(clk_125),  
    .clk_150(clk_150),  
    .datain(datain),  
    .start_transmission(start_transmission),  
    .ready_to_start(ready_to_start),  
    .destination_rdy(destination_rdy),  
    .numero_quartetti(numero_quartetti),  
    .cntf_databus(cntf_databus),  
    .cntf_wr_en(cntf_wr_en),  
    .led(leds[0])  
);  
  
// Control Module  
ModuloControllo modulo_controllo(  
    .clk(clk_150),  
    .data_bus(cntf_databus),  
    .datavalid(cntf_wr_en),  
    /*.startAcquisition(start_acquisition),  
    .start(start_acquisition),  
    .led(leds[2:1]),  
    .Amax(Amax),  
    .numero_quartetti(numero_quartetti)  
);  
  
ADC_MAX4800 ADC_MAX4800 (  
    .clk_50(clk_50),  
    .clk_150(clk_150),  
    .EN(start_acquisition),  
    .destination_rdy(destination_rdy),  
    .ready_to_start(ready_to_start),  
    /*.SDATA1(SDATA1),  
    .SDATA2(SDATA2),  
    .SDATA3(SDATA3),  
    .SDATA4(SDATA4),*/  
    .A0(A0),  
    .A1(A1),  
    .A2(A2),  
    .A3(A3),  
    .Amax(Amax),  
    .ClkADC(ClkADC),  
    /*.CS_n(CS_n),  
    .start_transmission(start_transmission),  
    .dataout(datain)  
);
```

Appendix B (Continued)

```
endmodule
```

The code below realizes the Ethernet interface between the FPGA control unit and the PC for system control and data acquisition and storage.

```
module ethernet(  
    input wire rst,  
    /*input wire duplex,*/  
    output reg PhyResetOut_pin,  
    //input wire MII_TX_CLK_pin, // 25 MHz clock for 100 Mbps - not used here  
    output reg [7:0] GMII_TXD_pin,  
    output reg GMII_TX_EN_pin,  
    output reg GMII_TX_ER_pin,  
    //output wire GMII_TX_CLK_pin,  
    input wire [7:0] GMII_RXD_pin,  
    input wire GMII_RX_DV_pin,  
    input wire GMII_RX_ER_pin,  
    input wire GMII_RX_CLK_pin,  
    output wire MDC_pin,  
    inout wire MDIO_pin,  
    input wire clk_125,  
    input wire clk_150,  
    input [31:0] datain,  
    output wire destination_rdy,  
    input [13:0] numero_quartetti,  
    output reg [31:0] cntf_databus,  
    output reg cntf_wr_en,  
    output reg led  
  
);  
  
reg send32  
assign destination_rdy = send32 & wr2_ready_i;  
  
wire wb_clk;  
assign wb_clk = clk_150;  
  
// Drive the GTX_CLK output from a DDR register  
wire GMII_GTX_CLK_int;  
  
// Register MAC outputs  
wire GMII_TX_EN, GMII_TX_ER;  
wire [7:0] GMII_TXD;  
  
always @(posedge GMII_GTX_CLK_int) begin  
    GMII_TX_EN_pin <= GMII_TX_EN;  
    GMII_TX_ER_pin <= GMII_TX_ER;  
    GMII_TXD_pin <= GMII_TXD;  
end  
  
// FIFOs are exposed for transferring data.  
localparam    dw = 32; // WB data bus width  
localparam    aw = 8; // WB address bus width
```

Appendix B (Continued)

```
reg      wb_rst = 0;
reg      rd2_ready_o, wr2_ready_o;
wire     wr2_ready_i, rd2_ready_i;
reg [3:0] wr2_flags;
reg [31:0] wr2_data;
wire [3:0] rd2_flags;
wire [31:0] rd2_data;

reg [dw-1:0] s6_dat_o;
wire [dw-1:0] s6_dat_i;
reg [aw-1:0] s6_adr;
wire s6_ack;
reg s6_stb, s6_cyc, s6_we;

reg txreset;
reg rxreset;

simple_gemac_wrapper #(.RXFIFOSIZE(9), .TXFIFOSIZE(6))
.txreset(txreset), .rxreset(rxreset),
.GMII_GTX_CLK(GMII_GTX_CLK_int), .GMII_TX_EN(GMII_TX_EN),
.GMII_TX_ER(GMII_TX_ER), .GMII_TXD(GMII_TXD),
.GMII_RX_CLK(GMII_RX_CLK_pin), .GMII_RX_DV(GMII_RX_DV_pin),
.GMII_RX_ER(GMII_RX_ER_pin), .GMII_RXD(GMII_RXD_pin),
.sys_clk(dsp_clk),
.rx_f36_data({rd2_flags,rd2_data}), .rx_f36_src_rdy(rd2_ready_i),
.rx_f36_dst_rdy(rd2_ready_o),
.tx_f36_data({wr2_flags,wr2_data}), .tx_f36_src_rdy(wr2_ready_o),
.tx_f36_dst_rdy(wr2_ready_i),
.wb_clk(wb_clk), .wb_rst(wb_rst), .wb_stb(s6_stb), .wb_cyc(s6_cyc),
.wb_ack(s6_ack),
.wb_we(s6_we), .wb_adr(s6_adr), .wb_dat_i(s6_dat_o), .wb_dat_o(s6_dat_i),
.mdio(MDIO_pin), .mdc(MDC_pin));

// Blast out some packets
(* fsm_encoding = "user" *)
reg [5:0] TXstate;

localparam TXready = 29;
localparam TX_ARP = 31;
localparam TX_UDP = 43;

(* fsm_encoding = "user" *)
reg [4:0] RXstate;

reg [25:0] count;
reg [5:0] rstcount;
reg [15:0] RXcount;
reg [15:0] TXcount;
reg [31:0] phy_status;
reg [4:0] phy_addr; // Valid for the Atlys

reg [15:0] databuf;

reg [15:0] UDP_length;
reg [15:0] UDP_lengthR;
reg [15:0] IP_length;
reg [15:0] IP_identification;

reg [47:0] SHA_buff;
reg [31:0] SPA_buff;
```


Appendix B (Continued)

```
// reg [31:0] TPA_buff;

reg response_ready;
reg response_started;

reg [47:0] DST_MAC = 48'h001e_ec8b_efd3;
reg [31:0] DST_IP = {8'd192, 8'd168, 8'd1, 8'd8};

localparam [47:0] SRC_MAC = 48'h0037_ffff_3737;
localparam [31:0] SRC_IP = {8'd192, 8'd168, 8'd1, 8'd10};

localparam [15:0] Type_ARP = 16'h0806;
localparam [15:0] HType = 16'h0001;
localparam [15:0] PType = 16'h0800;
localparam [7:0] HLen = 8'h06;
localparam [7:0] PLen = 8'h04;
localparam [15:0] Operation = 16'h0002;

reg [47:0] ARP_DST_MAC;
reg [31:0] ARP_DST_IP;
reg [28:0] arp_count;

parameter [15:0] SRC_PORT = 16'd59151;
parameter [15:0] DST_PORT = 16'd59150;

reg [31:0] tmpChecksum1;
reg [31:0] tmpChecksum2;
reg [15:0] rx_checksum;
reg [15:0] tx_checksum;
reg [15:0] check;

initial begin
    phy_status = 32'h0;

    TXstate = 6'd0;
    RXstate = 5'd0;

    count = 0;

    phy_addr = 7; //valid fo Atlys

    databuf = 16'd0;

    UDP_lengthR = 16'd0;
    UDP_length = 16'd0;
    IP_length = 16'd0;
    IP_identification = 16'h0001;

    txreset = 0;
    rxreset = 0;

    SHA_buff = 48'h0;
    SPA_buff = 32'h0;
    arp_count = 0;

end
```

Appendix B (Continued)

```
always @(posedge dsp_clk) begin

    arp_count = arp_count + 1;
    if(rst) begin
        IP_identification = 16'h0000;

        count = 26'h0;
        TXstate = 6'd0;
        led = 0;
    end
    else begin
        case(TXstate)
            0: begin
                PhyResetOut_pin = 1;
                wr2_ready_o = 0;

                wb_rst = 1;
                txreset = 1;

                send32 = 0;
                led = 0;
                ready_to_start = 0;

                count = count + 1'b1;
                if (count[23] == 1) begin
                    TXstate = TXstate+1;
                end
            end

            1: begin
                count = 26'h0;
                TXstate = TXstate+1;
            end

            2: begin
                PhyResetOut_pin = 0; // Active low reset
                count = count + 1'b1;
                if (count[23] == 1) begin
                    TXstate = TXstate+1;
                end
            end

            3: begin
                count = 26'h0;
                TXstate = TXstate+1;
            end

            4: begin
                PhyResetOut_pin = 1; // Bring out of reset, then wait for chip to
                fire up
                count = count + 1'b1;
                if (count[23] == 1) begin
                    TXstate = TXstate+1;
                end
            end

            5: begin
                wb_rst = 0;
                txreset = 0;
                s6_adr = 8'd20; // Set MDIO clock divider
                s6_dat_o = 32'd24; // to 24 (@150 = 6.25 MHz )
                s6_stb = 1;
            end
        endcase
    end
end
```

Appendix B (Continued)

```
s6_cyc = 1;
s6_we = 1;
TXstate = TXstate+1;

end
6: begin
if (s6_ack) begin
s6_stb = 0;
s6_cyc = 0;
s6_we = 0;
TXstate = TXstate+1;
end
end
7: begin
// First read the current status to make sure the PHY is present
s6_adr = {6'd6, 2'd0}; // ADDRESS =
s6_dat_o = {5'd1, 3'd0, phy_addr}; // Reg 1, NC, PHYADD n
s6_stb = 1;
s6_cyc = 1;
s6_we = 1;
TXstate = TXstate+1;
end
8: begin
if (s6_ack) begin
s6_stb = 0;
s6_cyc = 0;
s6_we = 0;
TXstate = TXstate+1;
end
end
9: begin
s6_adr = {6'd8, 2'd0}; // COMMAND =
s6_dat_o = 32'd2; // RSTAT
s6_stb = 1;
s6_cyc = 1;
s6_we = 1;
TXstate = TXstate+1;
end
10: begin
if (s6_ack) begin
s6_stb = 0;
s6_cyc = 0;
s6_we = 0;
TXstate = TXstate+1;
end
end
11: begin
s6_adr = {6'd9, 2'd0}; // Read MIISTATUS
TXstate = TXstate+1;
end
12: begin
if (~s6_dat_i[1]) begin // Wait until not busy
TXstate = TXstate+1;
end
end
13: begin
s6_adr = {6'd10, 2'd0}; // Read MIIRX_DATA
s6_we = 0;
s6_stb = 1;
s6_cyc = 1;
```

Appendix B (Continued)

```
        TXstate      = TXstate+1;
    end
14: begin
    if (s6_ack) begin
        s6_stb       = 0;
        s6_cyc       = 0;
        phy_status   = s6_dat_i;

        TXstate      = TXstate+1;
    end
end
15: begin
    // Set to GMII mode, first by reading reg 27
    s6_adr = {6'd6, 2'd0}; // ADDRESS =
    s6_dat_o = {5'd27, 3'd0, phy_addr}; // Reg 27
    s6_stb = 1;
    s6_cyc = 1;
    s6_we = 1;
    TXstate = TXstate+1;
end
16: begin
    if (s6_ack) begin
        s6_stb = 0;
        s6_cyc = 0;
        s6_we = 0;
        TXstate = TXstate+1;
    end
end
17: begin
    s6_adr = {6'd8, 2'd0}; // COMMAND =
    s6_dat_o = 32'd6; // RSTAT
    s6_stb = 1;
    s6_cyc = 1;
    s6_we = 1;
    TXstate = TXstate+1;
end
18: begin
    if (s6_ack) begin
        s6_stb = 0;
        s6_cyc = 0;
        s6_we = 0;
        TXstate = TXstate+1;
    end
end
19: begin
    s6_adr = {6'd9, 2'd0}; // Read MIISTATUS
    TXstate = TXstate+1;
end
20: begin
    if (~s6_dat_i[1]) begin // Wait until not busy
        TXstate = TXstate+1;
    end
end
21: begin
    // Now write to GMII mode register
    phy_status = s6_dat_i;
    s6_adr = {6'd6, 2'd0}; // ADDRESS =
    s6_dat_o = {5'd27, 3'd0, phy_addr}; // Reg 27
    s6_stb = 1;
    s6_cyc = 1;
```

Appendix B (Continued)

```
s6_we      = 1;
TXstate    = TXstate+1;
end
22: begin
  if (s6_ack) begin
    s6_stb   = 0;
    s6_cyc  = 0;
    s6_we    = 0;
    TXstate  = TXstate+1;
  end
end
23: begin
  s6_adr    = {6'd8, 2'd0}; // COMMAND = TxData
  s6_dat_o  = {phy_status[15:4], 4'b1111}; // HWCFG_MODE = GMII to Copper
  s6_stb    = 1;
  s6_cyc    = 1;
  s6_we     = 1;
  TXstate   = TXstate+1;
end
24: begin
  if (s6_ack) begin
    s6_stb   = 0;
    s6_cyc   = 0;
    s6_we    = 0;
    TXstate  = TXstate+1;
  end
end
25: begin

  s6_adr    = {6'd1, 2'd0}; // ADDRESS =
  s6_dat_o  = {16'd0, SRC_MAC[47:32]}; // Reg 1 - Unicast H
  s6_stb    = 1;
  s6_cyc    = 1;
  s6_we     = 1;
  TXstate   = TXstate+1;
end
26: begin
  if (s6_ack) begin
    s6_stb   = 0;
    s6_cyc   = 0;
    s6_we    = 0;
    TXstate  = TXstate+1;
  end
end
27: begin
  s6_adr    = {6'd2, 2'd0}; // ADDRESS =
  s6_dat_o  = SRC_MAC[31:0]; // Reg 2 - Unicast L
  s6_stb    = 1;
  s6_cyc    = 1;
  s6_we     = 1;
  TXstate   = TXstate+1;
end
28: begin
  if (s6_ack) begin
    s6_stb   = 0;
    s6_cyc   = 0;
    s6_we    = 0;
    TXstate  = TXready;
  end
end
```

Appendix B (Continued)

```
TXready: begin //Tx Ready State = 29
  ready_to_start = 0;
  count = 0;
// led = 0;
  if (arp_count > 29'd300_000_000) begin
    TXstate = TX_ARP;
    arp_count = 0;
  end else begin
    TXstate = TXready + 1;
  end
end
TXready + 1: begin
  ready_to_start = 1;
  if (start_transmission) begin
    UDP_length = 8+numero_quartetti*4; //UDP Length in byte
    IP_length = 28+2+numero_quartetti*4; //IP Length più i due byte
di padding
    tmpChecksum2 = 16'd0;
    TXstate = TX_UDP;
  end else begin
    TXstate = TXready;
  end
end
end

TX_ARP: begin
  ready_to_start = 0;
  ARP_DST_MAC = 48'h ffff_ffff_ffff;
  if (wr2_ready_i) begin
    wr2_flags = 4'b0001; //SOF: Start Of Frame
    wr2_data = ARP_DST_MAC[47:16];
    wr2_ready_o = 1;
    TXstate = TXstate+1;
    count = 0;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 1: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = {ARP_DST_MAC[15:0],SRC_MAC[47:32]};
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 2: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = SRC_MAC[31:0];
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
end
```

Appendix B (Continued)

```
end
TX_ARP + 3: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = {Type_ARP, HType};
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 4: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = {PType, HLen, PLen};
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 5: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = {Operation, SRC_MAC[47:32]};
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 6: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = SRC_MAC[31:0];
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 7: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = SRC_IP;
    wr2_ready_o = 1;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_ARP + 8: begin
  if (wr2_ready_i) begin
    wr2_flags = 4'b0000;
    wr2_data = SRC_MAC[47:16];
```

Appendix B (Continued)

```
        wr2_ready_o    = 1;
        TXstate       = TXstate+1;
    end else begin
        wr2_ready_o    = 0;
        wr2_flags      = 0;
    end
end
TX_ARP + 9: begin
    if (wr2_ready_i) begin
        wr2_flags      = 4'b0000;
        wr2_data        = {SRC_MAC[15:0], SRC_IP[31:16]};
        wr2_ready_o    = 1;
        TXstate         = TXstate+1;
    end else begin
        wr2_ready_o    = 0;
        wr2_flags      = 0;
    end
end
TX_ARP + 10: begin
    if (wr2_ready_i) begin
        wr2_data        = {SRC_IP[15:0],16'h0000};
        wr2_flags      = 4'b0010; //EOF: End Of Frame
        wr2_ready_o    = 1;
        TXstate         = TXstate+1;
    end else begin
        wr2_ready_o    = 0;
        wr2_flags      = 0;
    end
end
TX_ARP + 11: begin
    wr2_flags          = 0;
    wr2_ready_o        = 0;
    if (wr2_ready_i) begin
        count = count + 1;
    end
    if (count[6]) begin
        TXstate = TXready;
    end
end

TX_UDP: begin

    ready_to_start = 0;
    if (wr2_ready_i) begin
        tmpChecksum2 = DST_IP[15:0] + DST_IP[31:16];
        wr2_flags    = 4'b0001;
        = DST_MAC[47:16]; // dst mac (8)
        wr2_ready_o  = 1;
        count        = 0;
        TXstate      = TXstate+1;
    end else begin
        wr2_ready_o  = 0;
        wr2_flags    = 0;
    end
end
TX_UDP + 1: begin
    if (wr2_ready_i) begin
```


Appendix B (Continued)

```
tmpChecksum2 = tmpChecksum2 + SRC_IP[15:0] + SRC_IP[31:16];
wr2_flags    = 4'b0000;
wr2_data     = {DST_MAC[15:0],SRC_MAC[47:32]};
wr2_ready_o  = 1;
TXstate     = TXstate+1;
end else begin
    wr2_ready_o = 0;
    wr2_flags   = 0;
end
end
TX_UDP + 2: begin
    if (wr2_ready_i) begin
        tmpChecksum2 = tmpChecksum2 + 16'h0000 + 16'h4011; //poi Flags,
Offset e TTL,Protocol
        wr2_flags    = 4'b0000;
        wr2_data     = SRC_MAC[31:0]; // src mac (8)
        wr2_ready_o  = 1;
        TXstate     = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags   = 0;
    end
end
TX_UDP + 3: begin
    if (wr2_ready_i) begin
        tmpChecksum2 = tmpChecksum2 + 16'h4500; // protocol type ipv4
(1), header length (1) (*4), dsc (2)
        wr2_flags    = 4'b0000;
        wr2_data     = 32'h0800_4500; // hwtype ethernet (4), protocol type ipv4 (1),
header length (1) (*4), dsc (2)
        wr2_ready_o  = 1;
        TXstate     = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags   = 0;
    end
end
TX_UDP + 4: begin
    if (wr2_ready_i) begin
        tmpChecksum2 = tmpChecksum2 + IP_length + IP_identification;
        wr2_flags    = 4'b0000;
        wr2_data     = {IP_length , IP_identification}; //Total length e
Identification
        wr2_ready_o  = 1;
        TXstate     = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags   = 0;
    end
end
TX_UDP + 5: begin
    if (wr2_ready_i) begin
        tx_checksum = ~(tmpChecksum2[31:16] + tmpChecksum2[15:0]);
        wr2_flags    = 4'b0000;
        wr2_data     = 32'h0000_4011; // flags/frag offset (4), ttl (2), protocol
(2)
        wr2_ready_o = 1;
        TXstate     = TXstate+1;
    end else begin
        wr2_ready_o = 0;
    end
end
```

Appendix B (Continued)

```
        wr2_flags = 0;
    end
end
TX_UDP + 6: begin
    if (wr2_ready_i) begin
        wr2_flags = 4'b0000;
wr2_data = {tx_checksum, SRC_IP[31:16]}; //IP Checksum(4), Src IP(4)
        wr2_ready_o = 1;
        TXstate = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags = 0;
    end
end
TX_UDP + 7: begin
    if (wr2_ready_i) begin
        wr2_flags = 4'b0000;
        wr2_data = {SRC_IP[15:0], DST_IP[31:16]}; //Src IP(4), Dst IP(4)
        wr2_ready_o = 1;
        TXstate = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags = 0;
    end
end
TX_UDP + 8: begin
    if (wr2_ready_i) begin
        wr2_flags = 4'b0000;
        wr2_data = {DST_IP[15:0], SRC_PORT}; //Dst IP(4), Src Port(4)
        wr2_ready_o = 1;
        TXstate = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags = 0;
    end
end
TX_UDP + 9: begin
    if (wr2_ready_i) begin
        wr2_flags = 4'b0000;
        wr2_data = {DST_PORT, UDP_length};
        wr2_ready_o = 1;
        send32 = 1;
        TXstate = TXstate+1;
    end else begin
        wr2_ready_o = 0;
        wr2_flags = 0;
    end
end
TX_UDP + 10: begin
    if (destination_rdy) begin //destination_rdy = send32 & wr2_ready_i
        wr2_flags = 4'b0000;
        wr2_data = {16'h0000, datain[31:16]}; //UDP Checksum + 16bit Data
        databuf = datain[15:0];
        wr2_ready_o = 1;
        TXcount = 1;
        //TXstate = TXstate+1;
        send32 = 0;
        if (TXcount < numero_quartetti ) begin
            TXstate = TX_UDP + 11;
        end
    end
end
```

cioè fifo pronto e mi servono dati...

Appendix B (Continued)

```
        end else begin
            //send32 = 0;
            TXstate = TX_UDP + 12;
        end
    end else begin
        wr2_ready_o = 0;
        wr2_flags = 0;
    end
end

TX_UDP + 11: begin
    if (destination_rdy) begin
        if (TXcount < numero_quartetti ) begin
            wr2_flags = 4'b0000; //dati intermedi
            wr2_data = {databuf, datain[31:16]};
            databuf = datain[15:0];
            wr2_ready_o = 1;
            send32 = 0;
            TXcount = TXcount + 1;
        end
        else begin
            wr2_ready_o = 0;
            send32 = 0;
            TXstate = TXstate+1;
        end
    end else begin
        if (TXcount < numero_quartetti ) begin
            wr2_ready_o = 0;
            send32 = 1;
            wr2_flags = 0;
        end else begin
            wr2_ready_o = 0;
            send32 = 0;
            wr2_flags = 0;
            TXstate = TXstate+1;
        end
    end
end

if (destination_rdy) begin
    if (TXcount < numero_quartetti ) begin
        wr2_flags = 4'b0000; //dati intermedi
        wr2_data = {databuf, datain[31:16]};
        databuf = datain[15:0];
        wr2_ready_o = 1;
        send32 = 0;
        TXcount = TXcount + 1;
    end
    else begin
        wr2_ready_o = 0;
        send32 = 0;
        TXstate = TXstate+1;
    end
end else begin
    wr2_ready_o = 0;
    send32 = 1; basso;
    wr2_flags = 0;
end
end*/
```

Appendix B (Continued)

```
TX_UDP + 12: begin
  if (wr2_ready_i) begin
    wr2_data = {databuf, 16'd0};
    wr2_flags = 4'b0010;
    wr2_ready_o = 1;
    send32 = 0;
    TXstate = TXstate+1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
TX_UDP + 13: begin // tempo di IFG
  wr2_ready_o = 0;
  wr2_flags = 0;

  if (wr2_ready_i) begin
    count = count + 1'b1;
  end
  if (count[6]) TXstate = TXstate+1;
end
TX_UDP + 14: begin
  if (wr2_ready_i) begin
    wr2_ready_o = 0;
    wr2_flags = 0;
    send32 = 0;
    // led = 1;
    TXcount = 16'h0;
    TXstate = TXready;
    if (IP_identification == 16'hFFFF)
      IP_identification = 16'h0000;
    else
      IP_identification = IP_identification + 1;
  end else begin
    wr2_ready_o = 0;
    wr2_flags = 0;
  end
end
default: begin
  TXstate = 0;
end
endcase
end
end

always @ (posedge dsp_clk) begin
  if (rst) begin
    rxreset = 1;
    RXstate = 6'd0;
  end
  else begin
    case (RXstate)
      0: begin
        cntf_wr_en = 0;
        rd2_ready_o = 0;

        RXcount = 0;
      end
    end
  end
end
```

Appendix B (Continued)

```
if(rxreset == 1) begin
  if(rstcount == 14)begin
    rxreset = 0;
    rstcount = 0;
  end else begin
    rstcount = rstcount + 1;
  end
end
else begin
  RXstate = RXstate + 1;
end
end
1: begin
  rd2_ready_o <= 1;
  if(rd2_ready_i == 1 && rd2_flags == 4'b0001)begin
    SHA_buff[47:16] = rd2_data; //Destination MAC 32bit
    RXstate = RXstate + 1;
  end
end
2: begin
  if (rd2_ready_i == 1 ) begin
    SHA_buff[15:0] = rd2_data[31:16]; //Destination MAC 16bit
    //THA_buff[47:32] = rd2_data[15:0]; // Source MAC 16 bit
    RXstate = RXstate + 1;
  end
end
3: begin
  if (rd2_ready_i == 1 ) begin
    //THA_buff[31:0] = rd2_data; //Source MAC 32 bit
    RXstate = RXstate + 1;
  end
end
4: begin //siamo al campo EtherType, IPv4 = 0x0800 e ARP = 0x0806
  if (rd2_ready_i == 1 ) begin
    if(rd2_data[31:8] == 24'h080045) begin //se IPv4, Version(1), IHL(1),
ToS(2)
      tmpChecksum1 = {16'h0000,rd2_data[15:0]}; //Comincio a calcolare
il Checksum IP da confrontare con quello ricevuto
      RXstate = RXstate + 1; //stato che gestisce i
pacchetti UDP
    end else begin //Protocollo di comunicazione non implementato
      rxreset = 1;
      RXstate = 0;
    end
  end
end
5: begin //IP Length(4), Identification(4)
  if (rd2_ready_i == 1 ) begin
    tmpChecksum1 = tmpChecksum1 + rd2_data[31:16] + rd2_data[15:0];
    RXstate = RXstate + 1;
  end
end
6: begin //Flags, Offset, TTL, Protocol
  if (rd2_ready_i == 1 ) begin
    if(rd2_data[7:0] == 8'h11)begin
      tmpChecksum1 = tmpChecksum1 + rd2_data[31:16] + rd2_data[15:0];
      RXstate = RXstate + 1;
    end
  else begin
    rxreset = 1;
  end
end
```

Appendix B (Continued)

```
        RXstate = 0;
    end
end
end
7: begin //Checksum, Source IP
    if (rd2_ready_i == 1 ) begin
        tmpChecksum1 = tmpChecksum1 + rd2_data[15:0];
        check        = rd2_data[31:16];
        RXstate      = RXstate + 1;
    end
end
end
8: begin //Source IP, Dest IP
    if (rd2_ready_i == 1 ) begin
        SPA_buff[31:16] = rd2_data[15:0];
        tmpChecksum1 = tmpChecksum1 + rd2_data[31:16] + d2_data[15:0];
        RXstate      = RXstate + 1;
    end
end
end
9: begin //Dest IP, Source Port
    if (rd2_ready_i == 1 ) begin
        //SPA_buff[15:0] <= rd2_data[31:16];
        if({SPA_buff[31:16],rd2_data[31:16]}==SRC_IP) begin
            tmpChecksum1 = tmpChecksum1 + rd2_data[31:16];
            RXstate      = RXstate + 1;
        end
        else begin
            rxreset = 1;
            RXstate = 0;
        end
    end
end
end
10: begin
    if (rd2_ready_i == 1 ) begin //destPort, length
        if(rd2_data[31:16]==DST_PORT)begin//destPort, length
            rx_checksum = ~(tmpChecksum1[31:16] + tmpChecksum1[15:0]);
            UDP_lengthR = rd2_data[15:0] - 8;
            RXstate = RXstate + 1;
        end else begin
            rxreset = 1;
            RXstate = 0;
        end
    end
end
end
11: begin
    if (rd2_ready_i == 1 ) begin
        if(check == rx_checksum) begin
            cntf_wr_en = 1;
            cntf_databus = {16'h0000,rd2_data[15:0]};
            RXstate = RXstate + 1;
            RXcount = 1;
        end else begin
            rxreset = 1;
            RXstate = 0;
        end
    end
end
end
12: if (rd2_ready_i == 1 ) begin
    if(RXcount < UDP_lengthR[15:2]) begin
        cntf_wr_en = 1;
        cntf_databus = rd2_data;
    end
end
end
```

Appendix B (Continued)

```
        RXcount          = RXcount + 1;
    end else if(RXcount == UDP_lengthR[15:2]) begin
        cntf_databus     = (rd2_data >> (UDP_lengthR[1:0]*8));
        RXstate          = 0;
    end

    if(rd2_flags == 4'b0010) begin //EOF - end of frame
        RXstate = 0;
    end
end else begin
    cntf_wr_en = 0;
end
default: begin
    rxreset = 1;
    RXstate = 0;
end
endcase
end
end
endmodule
```

The overall control of the different modules is performed by the VHDL code listed below.

```
module ModuloControllo(
    input wire clk,
    input wire [31:0] data_bus,
    input wire datavalid,
    output start,
    output reg[1:0] led,
    input Amax,
    output [13:0] numero_quartetti
);

    reg startAcquisition;
    reg [7:0] state;
    reg [31:0] Counter;

    reg [7:0] buff[63:0];
    reg [5:0] readP;
    reg [5:0] writeP;
    reg [5:0] countP;

    localparam IDLE = 8'b0000_0000;
    localparam SET_VGA_GAIN = 8'b0000_0001;
    localparam SET_BOOSTER_GAIN = 8'b0000_0010;
    localparam SET_PULSE_T1 = 8'b0000_0011;
    localparam SET_PULSE_T2 = 8'b0000_0100;
    localparam SET_PULSE_T3 = 8'b0000_0101;
    localparam SET_NUMBER_OF_PULSES_CYCLE = 8'b0000_0110;
    localparam SET_CYCLE_HOLD_PERIOD = 8'b0000_0111;
    localparam START = 8'b0000_1000;

    localparam QUARTETS = 14'd360;
    assign numero_quartetti = QUARTETS;
```

Appendix B (Continued)

```
initial begin
state <= IDLE;
Counter <= 0;
buff[0] <= 0;
readP <= 0;
writeP <= 0;
countP <= 0;
led <= 2'b00;
startAcquisition <= 0;
end

always @ (posedge clk) begin
if(datavalid==1)begin
buff[writeP] <= data_bus[31:24];
buff[writeP+1] <= data_bus[23:16];
buff[writeP+2] <= data_bus[15:8];
buff[writeP+3] <= data_bus[7:0];
countP <= countP + 4;
writeP <= writeP + 4;
end
case(state)
IDLE:begin
startAcquisition <= 0;
if(countP>0)begin
case(buff[readP])
SET_VGA_GAIN : begin
state <= SET_VGA_GAIN;
end
SET_BOOSTER_GAIN : begin
state <= SET_BOOSTER_GAIN;
end
SET_PULSE_T1 : begin
state <= SET_PULSE_T1;
end
SET_PULSE_T2 : begin
state <= SET_PULSE_T2;
end
SET_PULSE_T3 : begin
state <= SET_PULSE_T3;
end
SET_NUMBER_OF_PULSES_CYCLE : begin
state <= SET_NUMBER_OF_PULSES_CYCLE;
end
SET_CYCLE_HOLD_PERIOD : begin
state <= SET_CYCLE_HOLD_PERIOD;
end
START : begin
state <= START;
end
default: begin
state <= IDLE;
end
endcase
readP <= readP + 1'b1;
if(datavalid==0)
countP <= countP - 1;
else
countP <= countP + 3;
end
end
end
```


Appendix B (Continued)

```
SET_VGA_GAIN : begin
    state <= IDLE;
end
SET_BOOSTER_GAIN : begin
    state <= IDLE;
end
SET_PULSE_T1 : begin
    state <= IDLE;
end
SET_PULSE_T2 : begin
    state <= IDLE;
end
SET_PULSE_T3 : begin
    state <= IDLE;
end
SET_NUMBER_OF_PULSES_CYCLE : begin
    state <= IDLE;
end
SET_CYCLE_HOLD_PERIOD : begin
    led <= 2'b10;
    state <= IDLE;
end
START : begin
    led <= 2'b11;
    startAcquisition <= 1;
    if (Amax == 1) begin
        state <= IDLE;
    end else begin
        state <= START;
    end
end
default: begin
    state <= IDLE;
end
endcase
end

BUF obuf_start (
    .I(startAcquisition),
    .O(start)
);

endmodule
```

Data acquisition from the 4 ADC modules is realized by the following VHDL

code.

```
`timescale 1ns / 1ps

module ADC_MAX4800(
    input wire clk_50,
    input wire clk_150,
    input wire EN,
    input wire destination_rdy,
    input wire ready_to_start,
    output wire A0,
```

Appendix B (Continued)

```
output wire A1,
output wire A2,
output wire A3,
output wire Amax,
output wire ClkADC,
output wire start_transmission,
output wire led_full,
output wire [31:0] dataout
);

wire clk_10, clk_16, clk_16_n;
wire SDATA1, SDATA2, SDATA3, SDATA4;

clk_ADC_MAXX4800 clock_generator (
    .clk_in1(clk_50),          // IN: 50 MHz
    .clk_out1(clk_10),        // OUT1: 10 MHz
    .clk_out2(clk_16),        // OUT2: 16 MHz
    .clk_out3(clk_16_n)       // OUT3: 16 MHz - negative
);

wire CS_n;

Serial_Data ADC_sim (
    .ClkADC(clk_16_n),
    .CS_n(CS_n),
    .SDATA1(SDATA1),
    .SDATA2(SDATA2),
    .SDATA3(SDATA3),
    .SDATA4(SDATA4)
);

TopModule ADC (
    .CLKin(clk_16),
    .CLKin_n(clk_16_n),
    .clk_50(clk_50),
    .clk_150(clk_150),
    .SDATA1(SDATA1),
    .SDATA2(SDATA2),
    .SDATA3(SDATA3),
    .SDATA4(SDATA4),
    .EN(EN),
    .CS_n(CS_n),
    .ClkADC(ClkADC),
    .A0(A0),
    .A1(A1),
    .A2(A2),
    .A3(A3),
    .Amax(Amax),
    .destination_rdy(destination_rdy),
    .start_transmission(start_transmission),
    .data_out(dataout),
    .ready_to_start(ready_to_start)
);

endmodule
```

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